9064

Datasheet

Issue	Draft01
Date	2025-10-15

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1 About This Document

1.1 Overview

This document describes the functionality, interfaces, signals, physical requirements, and the operating environment of 9064.

1.2 Audience

This document is for hardware, software, and application developers who need to understand 9064.

1.3 Revision History

Table 1-1 : Revision history

Date	Version	Description	Page
2025-10-15	Draft 01	First release for draft.	-

2 9064 Introduction

9064 is a leading purpose-built switch silicon that can be used to build high scalable, feature-rich versatile solution for ToR, Chassis Fabric Lane Card, Large Scale Enterprise and Campus Aggregation/Core chassis. 9064 supports up to 6.4Tbps I/O bandwidth and 2.7 BPPS core bandwidth. 9064 equips with 64 of SerDes Lanes. The device supports 10GE, 25GE, 40GE, 50GE, 100GE, 200GE, 400G, and 800G ports. There are two configuration modes of these 64 serdes lanes, the one is Mode A: 64x112G. The typical form factor of Mode A is 48x100G(R1) + 4x400G(R4) and the typical form factor for Mode B is 16x400G(R4).

The key features of 9064 are as bellow:

- 64 high-speed PAM4 SerDes with down compatibility with 25G/10G NRZ mode
- 64 lanes are 112Gbps rate.
- Full IPv4 and IPv6 dual stack routing
- ECN and PFC capability for RDMA lossless forwarding
- Low pin-to-pin forwarding latency
- 16MB embedded packet buffer with self-tuning threshold for more evenly and efficient buffer usage
- Enhanced on-chip Flow Tracing Engine for up to 128K flow table of NetFlow per packet-process engine and MMU engine
- Embedded Traffic manager providing 12 queue per port
- In-band Network Telemetry (INT) and In-band Flow Analyze (IFA) integration for Network Telemetry application
- Support Jumbo Frame up to 9600Bytes
- Improved PFC/WRED and headroom mechanism for lossless Ethernet
- Flexible forwarding database and policy-based table which can be configured to be different memory profile for different application
- Unused module can be power-off for power saving

The 9064 device family consists of multiple products, Table 2-1and Table 2-2 summarize the key difference in capabilities between the devices in 9064 device family.

Table 2-1 : 9064 Device Family

Device	SerDes CFG	Core Freq.	Wire Speed Packet Length	Package Size	Buffer
9064	64x112G	1.35G @ DP 1.4G @ PP	64B: 1.8T 128B: 3.1T	47.5mmx 47.5mm	16MB

			256B: 5.6T		

Table 2-2 : 9064 SerDes Configuration Mode

Mode	112G SerDes
A	48x100G-R1 + 4x400G-R4
B	16x 400G-R4

NOTE

All the SerDes lanes can be configured dynamic to lower speed.

3 Device Overview

3.1 Packet Process Pipeline Overview

3.1.1 Overview

9064, has enhanced the multi-slice packet process pipeline and the datapath architecture to improve the packet forwarding performance as well as to provide fixed and low latency.

The detailed packet process pipeline is as bellow.

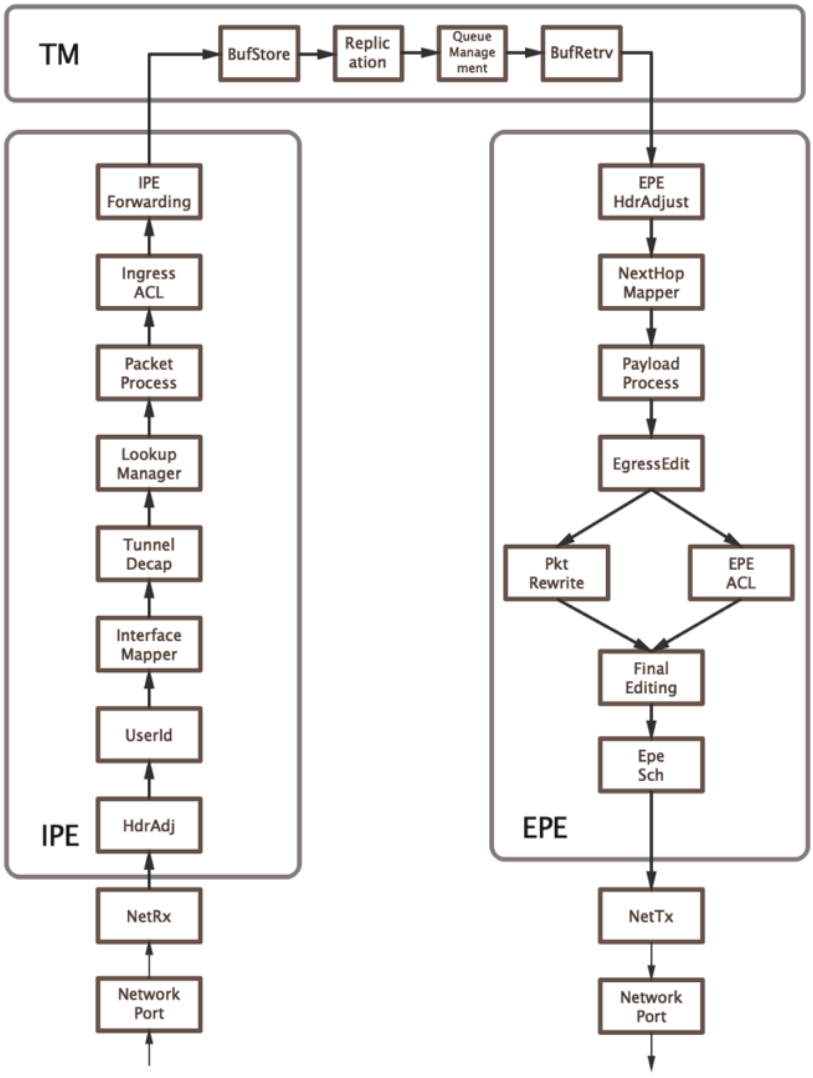

Figure 3-1 : The overview of Pipeline in each PP in 9064

3.2 Data-path Arch

The 9064 is based on multi-slice chip design where two DP engines are connected to one PP engine. The detailed block diagram is as bellow.

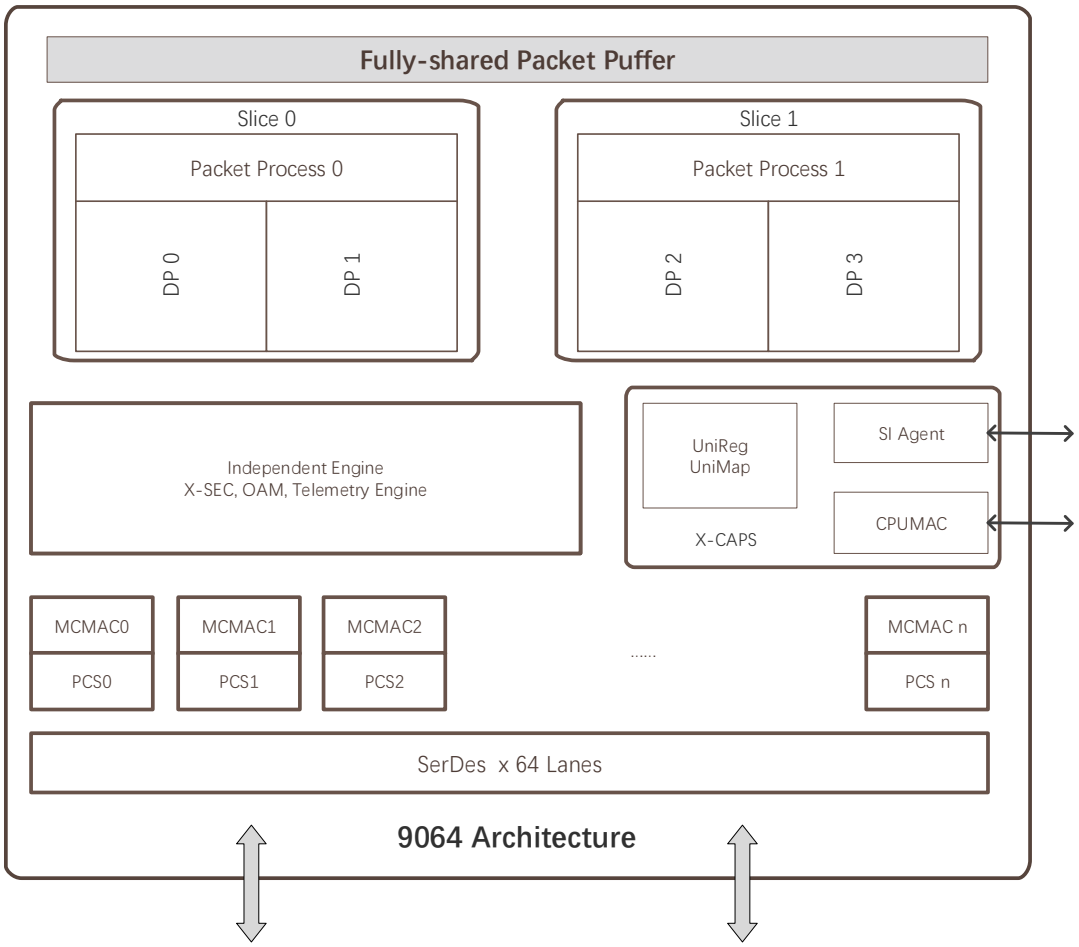

Figure 3-2 : Device Architecture Diagram

3.3 Feature List

Table 3-1 : Feature List

Feature	Description
CS SerDes Macro	16 CS Macros provide up to 64 SerDes lanes. Each lane can be configured to work at provide 10.3125G~112.5G lane speed with the following standards: • 800GbE: 800GBASE-CR, 800GAUI-8 • 400GbE: 400GBASE-KR8/CR8, 400GAUI-8; 400GBASE-KR4/CR4, 400GAUI-4 • 200GbE: 200GBASE-KR4/CR4, 200GAUI-4; 200GAUI-2, 200GBASE-CR2/KR2 • 100GbE: 100GAUI, 100GBASE-CR/KR, 100GAUI-2, 100GBASE-CR2/KR2, 100GAUI-4, CAUI-4, 100GBASE-CR4/KR4 • 50GbE: 50GBASE-KR2/CR2, 50GBASE-KR/CR, 50GAUI-2, 50GAUI • 40GbE (4-lane) 40GBASE-KR4/CR4, XLAUI, XLPPI • 25GbE: 25GAUI, 25GBASE-KR/CR

Feature	Description
	• 10GbE, XFI/ SFI, 10GBASE-KR/CR
Interface	10G/25G/40G/50G/100G/200G/400G/800Gbps speed, configured or auto-negotiated
	Standard MAC MIB
	Optional network port act as dedicated CPU traffic port
	X4 PCIe 3.0 for External CPU configuration and traffic interface **Notes:** The firmware of the eCPU needs to be upgraded to FW_V25.05 to support PCIe 3.0.
	CPU burst I/O access mode
	MDIO 1G/10G read/write/scan
	MAC LED
	I^2C Master Interface
	I^2C Slave Interface
L2 Bridging	SVL and IVL
	Hardware-based MAC learning and aging
	Station movement control
	Fast MAC flush per port/VLAN/port + VLAN
	Per VLAN / destination port controlled unknown discard for unicast /multicast / broadcast
	Unknown unicast/multicast/broadcast to CPU
	Static MAC
	Per port L2 protocol packet processing
	Port random log
	Access/trunk/hybrid port support
	Flexible AFT (per port accept/deny packets according to any combination of C-TAG and S-TAG)
	SW MAC learning and aging
	Black Hole MAC
	White List
	Dump MAC by port/ vlan / port+ vlan /MAC/MAC-fid
	Dump MAC by dynamic /static/all
	Dump MAC sort by trie tree
	Logic port learning for L2VPN
VLAN	Support C-VLAN and S-VLAN
	Global C-VLAN TPID and S-VLAN TPID setting and per port S-VLAN TPID selection
	Ingress and egress VLAN filtering
	Single or double tags VLAN translation on both ingress and egress
	Any combination of adding/replacing/removing operation for CVID /C-TAG CoS /

Feature	Description
	C-TAG CFI / SVID / S-TAG CoS / S-TAG CFI on both ingress and egress
	VLAN classification based on MAC SA/MAC DA/IP SA/IP DA/any L2 fields combination/protocol/port
	Single or double tag VLAN switching
	Private VLAN
	VLAN RX / TX statistics
	Spanning Tree, MSTP, RSTP
L2 Multicast	Per VLAN IGMP packet processing
	L2 multicast to physical port or tunnel
	PIM snooping
	Discard or send to CPU for unknown multicast packets
	IPDA, MACDA two level lookup
	IP base l2 multicast
Storm Control	Per port / VLAN storm control
	Both bits per second and packets per second rate limit
	Support unknown unicast /unknown multicast/ broadcast/ known unicast /known multicast /all unicast /all multicast rate limit
	Per MAC address rate limit
	Per port per packet type configurable threshold
Port LAG	Route Selection: • Static load balance for LAG • Regular and Random round-robin for LAG • Flowlet-based dynamic load balance for LAG • Resilient hashing for LAG • Forwarding mode for local members with higher priority • Load Balance Session Preservation
	Fault Tolerance: • Hardware-based LAG failover mechanism
Channel or CFlex LAG	Route Selection: • Static load balance for LAG • Regular and Random round-robin for LAG • Flowlet-based dynamic load balance for LAG • Resilient hashing for LAG • Load Balance Session Preservation
	Fault Tolerance: • Hardware-based LAG failover mechanism
ECMP	Route Selection: • Static load balance for ECMP • Regular and Random round-robin for ECMP • Dynamic load balance for ECMP • Resilient hashing for ECMP
	Fault Tolerance: • Hardware-based ECMP failover mechanism • Self-Healing for ECMP

Feature	Description
HASH mechanism	Fields for HASH: • L2: MAC SA / MAC DA / SVID / CVID / S-TAG CoS / C-TAG CoS/ EtherType • L3: IP DA/IP SA/IP header protocol/MPLS label • L4: TCP src/dest port, UDP src/dest port • Tunnel: Inner header's fields/outer header's fields/Inner+outer • Based on entropy information, for example: VXLAN, NVGRE, MPLS with entropy label
	Symmetric HASH
L3 Routing	4K Layer 3 interface, including VLAN interface and routed port
	Per L3 interface L3 protocol packet processing
	Per VLAN DHCP/ARP handling
	IPv4 and IPv6 host route
	Algorithm based IPv4 and IPv6 LPM (TCAM-based lookup is also supported)
	Public and Private route
	ECMP
	Loose and strict RPF check
	VRRP
	ICMP redirect check
	Virtual Route Forwarding, up to 8K instances
	uRPF
VXLAN	VXLAN Encap and Decap
	VXLAN Bridge and Routing
	VXLAN H-ECMP
	VXLAN Service Chain
Segment Routing	MPLS based Segment Routing
	IPv6 Based Segment Routing
IP Tunneling	Static V4inV4, V6inV4, V4inV6, V6inV6 tunnel
	6to4 tunnel
	GRE tunnel with Ethernet/IPv4/IPv6/MPLS/UserDefinedType as payload
	UDP tunnel
IP Overlay	VXLAN / NVGRE / VXLAN-GPE / GENEVE Support
IP Multicast Routing	(S, G), (*, G), (*, *) support
	Multicast RPF check
	Physical replication (to port) and logical replication (to VLAN)
	Fallback bridge on IPMC lookup failure
	Discard or send to CPU for unknown multicast packets
	PIM Sparse and Dense mode
	Bidirectional PIM
	Can be replicated to any port, VLAN, tunnel

Feature	Description
Network Security	Port/MAC based 802.1X
	Port Isolation • Per port isolation • Unidirectional and bidirectional • Isolation on flooded packets only or all packets
	Binding with any combination of IP/ MAC/ Port/ VLAN
	DDoS Attack Prevention for: • Illegal MAC SA • Illegal IP SA • Land Attack (MAC SA==MAC DA or IP SA==IP DA) • Null scan (TCP sequence number=0, control bits=0) • SYN/SYN-ACK flooding • Smurf attack
	Port/VLAN/System based MAC Limit
	Port Security
CPU Traffic Protection	Per protocol type rate limit
	Per group rate limit (multiple protocols can be grouped)
	4 priority classes with SP/FQ scheduling
	Total CPU traffic rate limit
	CoPP policing based on flow rules, with bps or pps
	Rate limit can be based on bps (bits per second) or pps (packet per second) unit
ACL	Both ingress and egress
	Applied on port, VLAN, L3Interface, and LogicPort
	24 parallel-lookup for ingress & 12 parallel lookup for egress ACL
	Deep packet parsing up to 192 bytes
	Match all L2-L4 fields UDF
	Actions supported: • Permit/deny • Redirect to port/L3 Nexthop/multicast group/tunnel • Redirect to CPU with timestamp attached • Mirror (port, L3 Nexthop, multicast group, tunnel, CPU) • Priority and color remark • Flow policing • Statistics • Add/remove/replace any fields in STAG and/or CTAG • Deny bridge • Deny learning • Deny routing • Random log to CPU • Select to on-chip flow tracing
	N-Flow™ technology
	Specify CPU Queue Id for traffic to CPU
	SGT

Feature	Description
	• Classify based on Port, VLAN, L3Interface and LogicPort • Flexible classify based on L2-L4 fields, and FIB • Support SGT encapsulation • Support SXP (identify and redirect to CPU)
	Class group-based ACL • Classify based on Port, VLAN, L3Interface and LogicPort • Flexible classify class group based on L2-L4 fields
	Policy based routing
	Forwarding Information as ACL key field
	Flexible ACL TCAM Allocation
Policing and QoS	SrTCM (RFC 2697) and modified TrTCM (RFC 4115)
	Support both color-aware and color-blind mode
	Fine granularity down to 8K bps
	Up to 16M Bytes burst size
	Support H-Policer at both IPE and EPE
	256 metering/policing profiles
	MEF 10.3 BWP
	Both ingress and egress policing
	Port/ Flow/ VLAN based policing
	PPS based policing
	Aggregated policing
	Meter action: discard, mark color, assign priority
	WRED congestion avoidance on per-queue basis, support arking for TCP traffic
	Tunnel ECN, flow-based ECN, stacking-based ECN
	CIR/PIR shaper with minimum guaranteed bandwidth and maximum regulated traffic for each queue.
	12 queue, 0,2,4,6 MC Queue Mode
	Configurable CIR/PIR weight, CIR is SP, PIR is SP/WFQ
	Traffic rate regulation for all destinations by FPS (frame per second) unit
	Ingress/Egress Resource Manage
	Flexible PHB Mapping
MPLS	Per system/per interface label space
	Full label space
	Penultimate Hop Pop
	L-LSP and E-LSP support
	Pipe/Short Pipe/Uniform Model LSP
	Parse/push/pop/lookup label number: 8/10/3/3
	Optimized Multi-Path MPLS, MPLS IP based ECMP
	Entropy label and flow label
	Martini Encapsulation

Feature	Description
	MPLS EVPN
	Raw mode and tagged mode PW
	VPWS (port AC, VLAN AC)
	VPLS (port AC, VLAN AC)/H-VPLS
	L3VPN
	Multicast MPLS
	Upstream MPLS
	MPLS over GRE Tunnel
	L2/L3 Gateway
	Using TCAM to resolve HASH conflict
Ethernet OAM	802.1ag Connectivity Fault Management
	Support both UP MEP and Down MEP, MIP
	CCM (interval 3.3ms/10ms/100ms/1s/60s/600s)
	Link Trace (LTM/LTR)
	Loopback (LBM/LBR)
	CSF/ AIS
	RDI
	APS/RAPS
	Link OAM
	802.3ah EFM
	Y.1731 Performance Measurement
	One-way/Two-way DM
	Single-end/Dual-end LM
	QinQ OAM
	VPLS/VPWS OAM
BFD	IP BFD
	LSP BFD
	VCCV/PW BFD
	VXLAN BFD
	NVGRE BFD
	S-BFD
	Micro-BFD
MPLS-TP OAM	Y.1731 based
	BFD based
Network Performance Management	RFC2544 for L2/L3
	Y.1564 for L2/L3
	TWAMP/OWAMP
	MEF SAT Testing (MEF46/MEF48/MEF49)

Feature	Description
	SLM/SLR
Automatic Protection Switch	Protocol/topology independent mechanism
	One-bit flap quick switch. No need to flush forwarding table
	2-level protection switch
	Support both unicast and multicast
	Support both source and sink end
	Can be comprehensively applied to G.8031/G.8032/G.8131/G.8132/IETF EAPS/Smart Link and all other possible protection switch protocols
	Hardware based APS switch
Mirror	Both ingress and egress mirror
	Port/VLAN/Flow based mirror
	32 mirror sessions
	Mirror destination: port/VLAN/tunnel/multicast group/CPU
	With extended information • Arrival timestamp • Forwarding latency • Application aware
	TCP session-sensed load balance
	Packet length truncation for log or to CPU
	Discard packet mirror • normal + discard mirror • only discard mirror
Network Time Synchronization	IEEE 1588-2008 with up to 4 management domains
	OC/BC/TC
	PTP over Ethernet/IPv4/IPv6
	G.8261 compliant Synchronize Ethernet with all SerDes capability
	SyncE reference selection
	Up to 2 SyncE clock output
	China Mobile ToD and sync interface
Address Translation	NAT
	NAPT
	NAT64: only support stateful NAT64
	TWICE NAT
Telemetry Engine	• Counter Sensor • MAC Stats • Enq/Deq Stats • ACL based stats • Buffer Depth Counter and Event Log • Global or port-based Latency Range Stats and log mechanism
	Path Sensor • INT: Standard INT, INT over UDP/TCP • INT enabling mechanism: flow based

Feature	Description
	• Multi-hop INT insertion capability • INT Postcard mode • IFA: support Live Traffic Mode and Clone Mode
	Hardware IP FIX(Flow Tracing） • Hardware Overlay Tunnel Learning • NetFlow Random Sampling and interval sampling • Hardware based aging • New Flow Export • First N packet for new flow log • Export based packet counter overflow or packet byte overflow or time expired or TCP session closed • Support IPFIX only when RPF Check Fail
DMA	Packet RX/TX • User Mode and Kernel Mode • SDK in User Mode, Packet TX/RX in Kernel
	DMA Info for IPFIX/Learning/Aging/Monitor
	DMA read/write table
	DMA Sync MAC stats
	HASH Dump
Truncation	Packet Truncation: port-based and flow-based

3.4 Target Application

3.4.1 ToR Switch

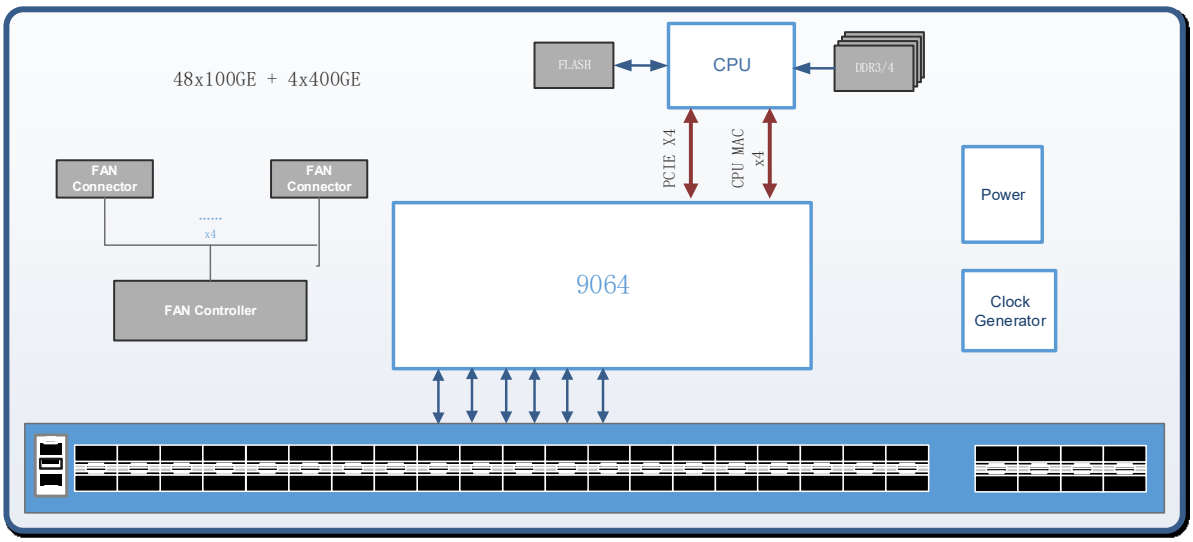

Figure 3-3 : 48x100G-R1 + 4x400G-R4

3.5 Highlights

- Low and fixed latency
- Advanced NetFlow capability
- SmartPort technology to provide a multitude of port speed
- Using CFlex Header stacking to address bandwidth cost of the CFlex Header
- Support In band telemetry, support INT and IFA protocol
- ECN and PFC for Lossless Ethernet

4 SmartPort Overview

4.1 9064 Architecture Overview

Figure 4-1 shows the data-path architecture of 9064. 9064 features 64 SerDes Lanes for network port. All of the Network port SerDes Lanes can be configured to work at 53.125G (PAM4) and can be downward-compatible with lower speed, 25.78125G (NRZ) and 10.3125G(NRZ). Meanwhile, there are 128 SerDes lanes can be configured to work at 112G bit rate. In addition, there are two independent SerDes Lanes can be configured to work as the connection between switch silicon and CPU Network Port.

CS SerDes Macro

- 8 Macros
  - 8 lanes per Macro
  - Multi-rate support
- 32Gbps to 112.5Gbps (PAM4)
- 10.3125G to 28.125 Gbps NRZ
- Support 10G/ 25G/ 40G/ 50G(2-lane and 1-lane)/100G(1-lane, 2-lane and 4-lane) / 200G(2-lane and 4-lane)/ 400G (4-lane and 8-lane)/ 800G(8-lane)
- 8 independent PLL to independently control speed of each lane

The 9064 features 2 Slice, each slice is with 2 data-path pipeline (DP) and 1 packet processing pipeline (PP). Each DP is equipped with 16 SerDes Lanes the detailed data-path pipeline is as bellow.

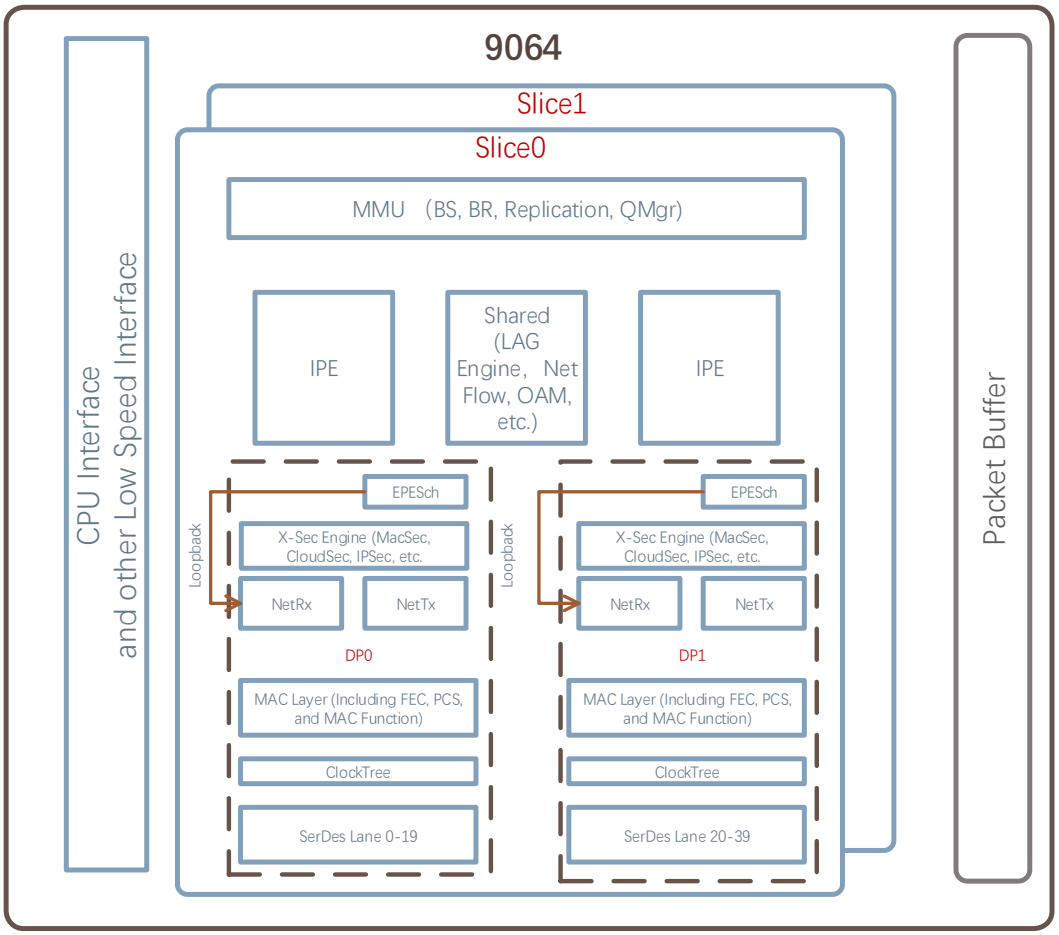

Figure 4-1 : 9064 chipset 4 Slices Arch

4.2 SerDes Macro Description

9064 integrates 8 CS SerDes Macros in the device for network ports. All of the SerDes Macros support NRZ and PAM4 date rate mode. The device features up to 64 SerDes lanes and 512 LocalPhyPort as known as network port.

Each lane in the SerDes macro support PN swap function to correct system wiring issues. Meanwhile, if the port is configured to work at multiple lane mode, the lane sequence relation can be modified according to the users' requirement. Note that, the lane sequence of RX and TX MUST be change as the same sequence pattern, for example the TX sequence of 100GE is 0->1->3->2, then the RX lane sequence MUST be 0->1->3->2 too.

The SerDes Macro in 9064 is compatible with multiple industry standards including:

- 10Gbps Ethernet application that include IEEE802.3ap and 10G-KR Ethernet over backplane
- 10Gbps Small Form Factor Module, XFP and XFI
- Enhanced 8.5 and 10Gigabit Small Form Factor Pluggable Module "SFP+", SFF-8431

- 25Gbps and 50Gbps Ethernet that include IEEE802.3by 25G BASE-KR Ethernet over back plane and 25G CR protocol and IEEE802.3cd 50G BASE-CR and 50GBASE-KR Ethernet over backplane
- 40Gbps and 100Gbps Ethernet applications that include IEEE802.3ba XLPPI/CPPI, XLAUI/CAUI CR4, KR4
- 100Gbps Ethernet application based on PAM4 mode and the SerDes lane rate is 106.25G include IEEE802.3CK 100GBASE-CR (Only CS SerDes supports)
- 200Gbps Ethernet application based on PAM4 mode, include IEEE 802.3bs 200GBASE-DR4/FR4/LR4 and 200GAUI-4, IEEE802.3cd 200GBASE-CR4 and 200GBASE-KR4 Ethernet over backplane and IEEE802.3CK 200GBASE-CR2 and 200GAUI-2(Only CS SerDes supports)
- 400Gbps Ethernet application include IEEE802.3bs 400GBASE-FR8/LR8 and 400GAUI-8, IEEE802.3CK 400GBASE-CR4 and 400GAUI-4 (Only CS SerDes supports)

4.2.1 SmartPort Group

9064's SmartPort architecture is designed to support dynamic port speed configuration, which enables customer to use the same silicon for different application scenarios.

In 9064, CS supports the lane rate from 10.3125G to 112.5G.

In 9064, 8 independent PLLs is integrated to independently control speed of each lane. SmartPort Configuration (Typical Formfactor) refer to 9064 table as bellow.

Table 4-1 : SerDes Macro

	XFI	XLAUI	25G	50G NRZ	50G PAM4	100G NRZ	100G PAM4	200G R4	400G R8	400G R4	800G R8
Lane0	XFI0	XLAUI0	25_0	50_0	50_0	100G_0	100G_0	200G_0	400G_0	400G_0	800G_0
Lane1	XFI1	XLAUI0	25_1	50_0	50_1	100G_0	100G_0	200G_0	400G_0	400G_0	800G_0
Lane2	XFI2	XLAUI0	25_2	50_1	50_2	100G_0	100G_1	200G_0	400G_0	400G_0	800G_0
Lane3	XFI3	XLAUI0	25_3	50_1	50_3	100G_0	100G_1	200G_0	400G_0	400G_0	800G_0
Lane4	XFI4	XLAUI1	25_4	50_2	50_4	100G_1	100G_2	200G_1	400G_0	400G_1	800G_0
Lane5	XFI5	XLAUI1	25_5	50_2	50_5	100G_1	100G_2	200G_1	400G_0	400G_1	800G_0
Lane6	XFI6	XLAUI1	25_6	50_3	50_6	100G_1	100G_3	200G_1	400G_0	400G_1	800G_0
Lane7	XFI7	XLAUI1	25_7	50_3	50_7	100G_1	100G_3	200G_1	400G_0	400G_1	800G_0

5 Memory Profile

9064 incorporates eTCAM and eSRAM as table memory. FTM technology enables flexible table memory partition per customer requirement. Each table size combination is called as a “memory profile”. On chip memory resources such as TCAM and embedded SRAM are considered as a sharing pool. With different memory profiles, the chip is able to support different cases such as more MAC address or more IP address. Table 5-1 shows example of memory profiles supported by 9064.

Table 5-1 : Typical 9064 FTM profiles

Table	Max	Lane Card
MAC	352K	223K
IP Host	32K	32K IPv4 + 32K IPv6
LPM (v4)	640K	128K IPv4 +128K Ipv6
Flow HASH	256K	256K
SCL0	40K per PP 32K per PP (AD)	40K per PP 32K per PP(AD)
SCL1	16K per PP 16K per PP(AD)	
EgressSCL0/1	16K/16K	16K/16K per PP
ACL(Ing/Egr)	48K/3K	48K/3K
OAM	4K	4K
L2MC	120K	4K
L3MC	120K	32K
NextHop	160K	96K

6 System Interface

6.1 Overview

9064 integrates the following major external interfaces:

- Multiple Speed SerDes Lanes, work as Network Interface
- I^2C Master Interface to access the external Optical Modules
- I^2C Slave Interface to communicate with external CPU
- PTP and Sync-E Interface for time synchronization and IEEE protocol
- SMI, IEEE802.3-compliant Serial Management Interface for communication with external PHY devices
- PCIe 3.0 (The firmware of the eCPU needs to be upgraded to FW_V25.05 to support PCIe 3.0.)

6.2 Network Interface

18 octal HSS Macros are integrated in 9064 for network ports. These SerDes lanes support multiple speeds for multiple port standards. The following table shows the different port speed mode supported by the SerDes lanes integrated in 9064.

Port Speed	Interface Type	Physical Planes	FEC Mode	Signaling Mode	SerDes Lane Bit Rate
800G	800GAUI-8 800GBASE-KR8/CR8	8	RS(544,514) RS(272,257)	53.125G PAM4	106.25G
400G	400GAUI-4 400GBASE-KR4/CR4	4	RS(544,514) RS(272,257)	53.125G PAM4	106.25G
	400GAUI-8 (C2C, C2M) 400GBASE-KR8/CR8	8	RS(544,514) RS(272,257)	26.5625G PAM4	53.125G
200G	200GAUI-4 (C2C, C2M) 200GBASE-KR4/CR4	4	RS(544,514) RS(272,257)	26.5625G PAM4	53.125G
	200GAUI-2 200GBASE-KR2/CR2	2	RS(544,514) RS(272,257)	53.125G PAM4	106.25G
100G	100GBASE—KR/CR	1	RS(544,514) RS(277,257) Interleaved FEC	53.125G PAM4	106.25G
	100GBASE-KR4/CR4 CAUI-4	4	RS(544,514)	26.5625G NRZ	26.5625G
		4	RS(528,514)	25.78125G NRZ	25.78125G
		4	None	25.78125G NRZ	25.78125G

Port Speed	Interface Type	Physical Planes	FEC Mode	Signaling Mode	SerDes Lane Bit Rate
	100GBASE-KR2/CR2 CAUI-2	2	RS(544,514)	26.5625G PAM4	53.125G
		2	RS(272,257)	26.5625G PAM4	53.125G
		2	RS(528,514)	25.78125G PAM4	51.5625G
		2	None	25.78125G PAM4	51.5625G
50G	50GBASE-KR2/CR2	2	RS(544,514)	26.5625G NRZ	26.5625G
		2	RS(528,514)	25.78125G NRZ	25.78125G
		2	None	25.78125G NRZ	25.78125G
	50GBASE-KR/CR	1	RS(544,514)	26.5625G PAM4	53.125G
		1	RS(272,257)	26.5625G PAM4	53.125G
		1	RS(528,514)	25.78125G PAM4	51.5625G
		1	None	25.78125G PAM4	51.5625G
40G	40GBASE-KR4/CR4, XLAUI	4	FC(2112,2080)	10.3125G NRZ	10.3125G
		4	None	10.3125G NRZ	10.3125G
25G	25GBASE-KR/CR, 25GAUI	1	RS(528,514)	25.78125G NRZ	25.78125G
		1	FC(2112,2080)	25.78125G NRZ	25.78125G
		1	None	25.78125G NRZ	25.78125G
10G	10GBASE-KR/CR, XFI	1	FC(2112,2080)	10.3125G NRZ	10.3125G
		1	None	10.3125G NRZ	10.3125G

6.2.1 Interface Signal

Table 6-1 : Interface Signal

Pin Name	Type	Rate	Pin#	Description
CS Group Interface				
CS[00:07]_RX_P[7:0] CS[00:07]_RX_N[7:0] CS[00:07]_RX_P[7:0] CS[00:07]_RX_N[7:0]	CML IN	10.3125G~ 112.5Gbps	256	10.3125G~112.5Gbps SerDes links input Typical configurations are: • XFI/SFI/10GBASE-KR/10.3125Gbps • XLAUI/40GBASE-KR4/CR4 • 25GAUI/25GBASE-KR/CR,25.78125Gbps • 50GAUI-2/50GBASE-CR2/KR2, 25.78125Gbps/26.5625 (NRZ) • 100GBASE-CR4/KR4/CAUI-4, 25.78125Gbps/26.5625 (NRZ) • 50GAUI-1/50GBASE-CR/KR,26.5625Gbps/25,78125 (PAM4) • 100GAUI/100GBASE-CR2/KR2, 25.78125Gbps/ 26.5625Gbps (PAM4) • 200GAUI-4/200GBASE-CR4/KR4, 26.5625G

Pin Name	Type	Rate	Pin#	Description
				• 400GAUI-8/400GBASE-CR8/KR8, 26.5625G • 100GAUI/100GBASE-CR/KR, 53.125G • 200GAUI-2/200GBASE-CR2/KR2, 53.125G • 400GAUI-8/400GBASE-CR8/KR8, 53.125G • 800GAUI-8/800GBASE-CR8/KR8, 53.125G
CS[00:07]_TX_P[7:0] CS[00:07]_TX_N[7:0] CS[00:07]_TX_P[7:0] CS[00:07]_TX_N[7:0]	CML OUT	10.3125G - 112.5G	256	10.3125G~112.5Gbps SerDes links output

6.2.2 10GE Ports

10 Gigabit MAC Standard Features

- Compliant to IEEE Std 802.3-2012 Clause 46, 47, 48, 49

10 Gigabit MAC Extended Features

- MAC/ RS/ PCS implementations compliant to IEEE 802.3 specifications
- Comprehensive statistics gathering with statistic vector outputs
- Supports flow-control in both directions
- Per frame and default programmable padding and FCS insertion
- Supports Deficit Idle Count for maximum data throughput
- Maintains minimum IFG under all conditions and provides line rate performance
- XGMII local and remote link fault detection and generation
- Supports loopback for diagnose
- Supports backplane auto-negotiation and link training
- Supports Base-R FEC (FC (2112,2080))

Supports IEEE 802.3az for 10Gbps operation Basic Operation

The SGMAC module performs the packet transmission and reception protocol as described in IEEE standard 802.3-2012 including a MAC Control Sub-layer and PCS layer.

In transmitting direction, the SGMAC module receives data from internal data bus and performs idle conversion, code group generation 64b/66b encoding for XFI/SFI/10G-KR. Next, the SGMAC prepares the data for transmission over one link for XFI/SFI/10G-KR.

In receiving direction, the SGMAC module 1-lane data for XFI/SFI/10G-KR from a SerDes lane.

6.2.3 40GE Ports

40 Gigabit MAC Standard Features

- Compliant to IEEE Std802.3-2012 Clause 80~83

40 Gigabit MAC Extended Features

- MAC/RS/PCS implementations compliant to IEEE 802.3 specifications
- Supports flow-control in both directions
- Per frame and default programmable padding and FCS insertion
- XLGMII local and remote link fault detection and generation
- Supports Deficit Idle Count for maximum data throughput
- Maintains minimum IFG under all conditions and provides line rate performance
- Supports backplane auto-negotiation and link training
- Supports Base-R FEC (FC (2112,2080))

Basic Operation

The XLGMAC module performs the packet transmission and reception protocol as described in IEEE standard 802.3ba.

In transmitting direction, the XLGMAC module receives data from internal data bus and performs idle conversion, code group generation, and 64b/66b encoding for XLAUI. After that, the XLGMAC prepares the data for transmission over 4 links for XLAUI.

In receiving direction, the XLGMAC module accepts 4-lane wide data for XLAUI from four lines of SerDes. XLGMAC pass data to 64b/66b decoding, then go to the XLGMII data bus.

During operation, the XLGMAC collects statistics about the success and failure of various operations. The statistic information is processed by network management entities in the system.

6.2.4 25GE Ports

25 Gigabit MAC Standard Features

- Compliant to IEEE Std802.3by
- Compliant to 25G&50G Ethernet Consortium Specification Rev1.6

25 Gigabit MAC Extended Features

- MAC/RS/PCS/FEC implementations compliant to IEEE 802.3 by and 25G&50G Consortium specifications
- Supports both RS-FEC (RS (528,514)) and Base-R FEC (FC (2112,2080))
- Supports flow-control in both directions
- Per frame and default programmable padding and FCS insertion
- 25GMII local and remote link fault detection and generation
- Supports Deficit Idle Count for maximum data throughput
- Maintains minimum IFG under all conditions and provides line rate performance
- Supports IEEE Clause 73 backplane auto-negotiation and link training

Basic Operation

The 25GMAC module performs the packet transmission and reception protocol as described in IEEE standard 802.3by or 25G&50G Consortium.

In transmitting direction, the 25GMAC module receives data from internal data bus and performs idle conversion, code group generation, and 64b/66b encoding for 25GAUI. After that, the 25GMAC prepares the data for transmission over one link for 25GAUI.

In receiving direction, the 25GMAC module accepts one lane data for 25GXAUI from one line of SerDes. 25GMAC pass data to 64b/66b decoding, then go to the 25GMII data bus.

During operation, the 25GMAC collects statistics about the success and failure of various operations. The statistic information is processed by network management entities in the system.

6.2.5 50GE Ports

50 Gigabit MAC Standard Features

- Compliant to 25G&50G Ethernet Consortium Specification Rev1.6

50 Gigabit MAC Extended Features

- MAC/RS/PCS/FEC implementations compliant to 25G&50G Consortium specifications
- Supports RS-FEC (RS (528,514)), RS-FEC (RS (544,514)), RS-FEC (RS (272,257)) and Base-R FEC (FC (2112,2080))
- Supports flow-control in both directions
- Per frame and default programmable padding and FCS insertion
- 50GMII local and remote link fault detection and generation
- Supports Deficit Idle Count for maximum data throughput

- Maintains minimum IFG under all conditions and provides line rate performance
- Supports backplane auto-negotiation and link training

Basic Operation

The 50GMAC module performs the packet transmission and reception protocol as described in 25G&50G Consortium.

In transmitting direction, the 50GMAC module receives data from internal data bus and performs idle conversion, code group generation, and 64b/66b encoding for 50GAUI. After that, the 50GMAC prepares the data for transmission over one/two links for 50GAUI.

In receiving direction, the 50GMAC module accepts 1-lane/2-lane wide data for 50GXAUI from two lines of SerDes. 50GMAC pass data to 64b/66b decoding, then go to the 50GMII data bus.

During operation, the 50GMAC collects statistics about the success and failure of various operations. The statistic information is processed by network management entities in the system.

6.2.6 100GE Ports

100 Gigabit MAC Standard Features

- Compliant to IEEE Std802.3-2012 Clause 80~83
- Compliant to 25G Ethernet Consortium Specification

100 Gigabit MAC Extended Features

- MAC/RS/PCS/FEC implementations compliant to IEEE 802.3 specifications
- Supports 100G RS-FEC (RS (528,514))
- Supports 100G RS-FEC (RS (544,514)) and RS-FEC (RS (272,257))
- Supports flow-control in both directions
- Per frame and default programmable padding and FCS insertion
- CGMII local and remote link fault detection and generation
- Supports Deficit Idle Count for maximum data throughput
- Maintains minimum IFG under all conditions and provides line rate performance
- Supports backplane auto-negotiation and link training

Basic Operation

The CGMAC module performs the packet transmission and reception protocol as described in IEEE standard 802.3bj and IEEE standard 802.3cd.

In transmitting direction, the CGMAC module receives data from internal data bus and performs idle conversion, code group generation, and 64b/66b encoding for

CAUI. After that, the CGMAC prepares the data for transmission over 4 links for CAUI.

In receiving direction, the CGMAC module accepts 4-lane wide data for CAUI from four lines of SerDes. CGMAC pass data to 64b/66b decoding, then go to the CGMII data bus.

During operation, the CGMAC collects statistics about the success and failure of various operations. The statistic information is processed by network management entities in the system.

6.2.7 200GE Ports

There are total 8 Multiple-Speed MACs integrated in 9064 to provide up to 8x200GbE ports. The embedded 200GE ports have the following features:

- IEEE 802.3 200GBASE-R PCS and 200GMII compliance
- Support RS-FEC (544,514) and RS-FEC (RS (272,257))
- FCS generation for transmitting, checking for receiving packets
- Includes PCS block (64b/66b) for SerDes interface.

Basic Operation

9064 implements a MAC unit with PCS layer integrated. It can be programmed to filter out frames that are longer or shorter than specific sizes. It also filters packets out with bad CRCs or reception error.

- Enable/Disable Port
- MAC Speed
- IEEE 802.3x Flow Control
- Link State
- Enable/Disable CRC Checking
- Maximum Receive Unit (MRU)
- The SerDes link runs at 53.125Gbps.

6.2.8 400GE Ports

There are total 4 Multiple-Speed MACs integrated in 9064 to provide up to 4x400GbE ports. The embedded 200GE ports have the following features:

- IEEE 802.3 400GBASE-R PCS and 400GMII compliance
- Support RS-FEC (544,514) and RS-FEC (RS (272,257))
- FCS generation for transmitting, checking for receiving packets
- Includes PCS block (64b/66b) for SerDes interface.

Basic Operation

9064 implements a MAC unit with PCS layer integrated. It can be programmed to filter out frames that are longer or shorter than specific sizes. It also filters packets out with bad CRCs or reception error.

- Enable/Disable Port
- MAC Speed
- IEEE 802.3x Flow Control
- Link State
- Enable/Disable CRC Checking
- Maximum Receive Unit (MRU)
- The SerDes link runs at 53.125Gbps.

6.3 Embedded Co-processor Interface

Four of RSIC-V based CPU cores are integrated in 9064 to work as a co-processor in 9064. ECPU supports the following functions:

- Internal registers access: direct access and DMA access
- Message/Packet TX/RX
- Operation acceleration of software learning

6.3.1 UART Interface

UART Interface is integrated as serial port connected to embedded ECPU and MCU in Port/MAC related module. Two UART interfaces are integrated in 9064. One is connected to ECPU and the other is connected to MCU in Port/MAC module.

Detailed function is as bellow:

- Configurable data-width: 5, 6, 7, and 8 bits.
- Configurable baud rate: 9600/…/115200/230400.
- Configurable check bit: even, odd, sticky, or no-parity check mode.
- Configurable stop-bit: 1bit or 2bit stop bit generation.

Table 6-2 : UART Interface Signal

Name	Type	Description
UART_TXD[1:0]	O, SDIO	Output Data of UART interface, 5Mbps
UART_RXD[1:0]	I, SDIO	Input Data of UART interface, 5Mbps

6.3.2 QSPI Interface

QSPI, Quad Serial Peripheral Interface, is used to provide the external FLASH access interface to embedded ECPU of 9064. QSPI interface in 9064 is compatible with

Motorola SPI specification. QSPI in 9064 can support 1-bit, 2-bit, and 4-bit data width. QSPI in 9064 can support PIO and PP work mode. The data transferring rate can support user-define mode.

Embedded ECPU support auto-boot mode. Under this mode, only first 16MB address space is used to store the boot up image. When the auto-mode is enabled, ECPU load the image from external NOR Flash and need to finish the running software in the external NOR Flash after self-check in system bootup is finished. This operation above is processed automatically without any configuration by external CPU.

Table 6-3 : QSPI Interface Signal

Name	Type	Description
QSPI_CLK	O, SDIO	QSPI clock signal, 22.5MHz and 6MHz is supported by default. The frequency is controlled by the pin QSPI_CLK_DIV_SEL.
QSPI_CSB[1:0]	O, SDIO	QSPI chip select signal
QSPI_DATA[3:0]	InOut, SDIO	QSPI bidirectional data
QSPI_CLK_DIV_SEL	Input	QSPI Clock Select If QSPI_CLK_DIV_SEL = 1, the Clock Frequency of QSPI is 5.9375MHz. Else, the Clock Frequency is 23.75MHz.

6.3.3 PCIe Interface

The quad SerDes is dedicated for CPU interface which support up to PCIe GEN3 data rate, 4 x 8Gbps. The data rate is auto negotiated during PCIe training. The PCIe could be used for register configuration, tables DMA, and packet data transferring.

The PCIe related interface signal is as bellow:

Table 6-4 : PCIe Interface Signal

Name	Type	Description
PCIE_REFCLK_P PCIE_REFCLK_N	HCSL	PCIe input deferential reference clock 100M.
PCIE_RXP[3:0] PCIE_RXN[3:0]	I CML	PCIe input data.
PCIE_TXP[3:0] PCIE_TXN[3:0]	O CML	PCIe output data.
PCIE_FORCE_RATE[1:0]	I LVCMOS	PCIe force mode: 2'b00: No Force mode; 2'b01: Force to Gen1; 2'b10: Force to Gen2; 2'b11: Force to Gen3;

Name	Type	Description
PCIE_FORCE_WIDTH[1:0]	I LVCMOS	PCIe Force Width 2'b00: x4(default); 2'b01: x1; 2'b10: x2; 2'b11: same as 2'b00
PCIE_REFCLK_LOGIC_SEL [1:0]	I LVCMOS	0x00: PCIe reference clock mode selection; Pull-down resisters are recommended
PCIE_RXCLK_PU	I LVCMOS	chip power up, active high, (for REFCLK_RX_CLKDET)
PCIE_REFCLK_VCM_SEL	Input	Pull-down resister is recommended
PCIE_REFCLK_EXT_SEL	I LVCMOS	Pull-down resister is recommended
PCIE_REFCLK_RX_RDY	O LVCMOS	If assert, indicate PCIe reference clock is ready.
PCIE_ANAGRP_PU	I LVCMOS	For CHIP power up, active high.

For PCIe bring-up and link training, the external NOR Flash is necessary. When boot-up processing, the FW of PCIe is loaded to internal RAM for PCIe bring-up. The RISC-V CPU ECPU-0 is used for PCIe bring-up. The ECPU load the boot-up FW from external NOR Flash and into the internal RAM. After the firmware being loaded successfully, the PCIe jumps to Link Training course. If the PCIe link training is finished, the BOOT_DONE is asserted. Then the CORE_RST_B pin needs to be released to begin the initialization of switch core.

6.4 I²C Master/Slave Interface

9064 supports serial bus interface which is compatible with Philips I²C standards. The master and slave function are supported on separated interfaces.

The I²C slave interface is used for slow speed configuration for internal register or table. In most cases the I²C slave interface is used to configure the PCIe interface speed and number of lanes. In addition, the junction temperature and core voltage could be read through the I²C slave bus.

The address LSB 2 bits of 9064 I²C slave interface is configurable by tie 2 external pins to VDD or GND. So the I²C slave address is 7'b011_11??. For 7bits address mode and for 10 bits address mode, the address is 10'b00_0011_11??.

The I²C master interfaces do not support clock synchronizing/stretch function, and can only be used to access the external optical modules such as XFP, SFP +. The state of external optical modules could be collected by I²C master interface periodically and save to internal 256Bytes memory.

The I²C slave/Master interface supports the speed no more than 400KHz.

6.5 JTAG Interface

A traditional JTAG provides the capability to test for short and open conditions when the device is mounted in the PCB based on a direct connection. In 9064, JTAG is used to connect the PCIe and embedded CPU in 9064. Only one module can be connected and controlled simultaneously.

Table 6-5 : JTAG Interface Signal

Name	Type	Description
TDO	O, SDIO	JTAG data output
TCK	I, SDIO	JTAG clock input
TDI	I, SDIO	JTAG data input
TMS	I, SDIO	JTAG test mode select input
TRST_B	I, SDIO	JTAG test reset, active low

6.6 PTP and Sync Ethernet Interface

9064 supports packet-based Time Synchronization (IEEE1588 and IEEE802.1AS) and Synchronous Ethernet Layer-one Clock Recovery (ITU G.8261). The synchronous communication over Ethernet is a control protocol that negotiates resource and timing on the network. The protocol synchronizes the real-time clocks in a system and enables network measurement and control based on real time.

6.6.1 Sync Ethernet Interface

The sync Ethernet interface provides the scheme to recover the clock from upstream devices and pass the clock to downstream devices through physical layer. 9064 generates four output clocks to feed in an external DPLL to produce transmitting reference clock. These four clocks are divided into two groups. Each group corresponds to 6 HSS Macro.

Table 6-6 : Sync Ethernet Signals

Name	Type	Description
RECV_CLK[1:0]	O, SDIO	SyncE recovery Clock

The corresponding relationship between the RECV_CLK and SerDes Macro is as bellow:

- RECV_CLK0: All SerDes Macros
- RECV_CLK1: All SerDes Macros

The detailed recovery clock frequency of different ports speed is as Table 10-5.

6.7 SMI Interface

9064 supports the IEEE 802.3 MII Management Interface via the MDIO and MDC pins. MDIO is a serial input and output data signal which is clocked by the periodic clock MDC. This interface allows 9064 accesses to the PHY internal registers, by which 9064 can monitor and control the real-time status of the external PHY devices connected to 9064.

Besides, SMI interface could scan the state of PHY devices continuously without CPU involved to collect the link status. It will trigger the APS operation while there are failures of links.

Table 6-7 : SMI Interface Signals

Name	IO	Description
MDC_A[3:0] MDC_B[3:0]	O LVCMOS	External PHY MDIO clock.
MDIO_A[3:0] MDIO_B[3:0]	I/O LVCMOS	External PHY MDIO data.
MDIO_A_VDDIO_SEL MDIO_B_VDDIO_SEL	I LVCMOS	Configured PIN to select the related voltage of I/O pin. 1: 1.2V NC: 1.8V

6.7.1 Operation

Though each SMI interface can support up to 32 PHY devices, 9064 provides 2 groups to mitigate the load to reduce the system design difficulty.

There are two operation types for SMI interface operation, the one is read/write operation, the other is auto-scan. The read/write operation can only access one register one time, but the auto-scan can access multiple status registers of many PHY.

6.8 LED Interface

The serial LED interface consists of encoded bit stream. The timing and encoding diagram are shown in the following figure. An EPLD or simple shift register logic is needed to convert this bit stream to drive individual LED.

The port sequence is programmable through internal register. Every port supports 2 modes: On/Off mode and Blink mode. Every port can be configured to support 1 mode (only one LED for one MAC) or 2 modes (there are 2 LEDs for one MAC) independently. If 1 mode is configured, then this port only output 1 bit on LED interface; If mode 2 is configured, then this port output 2 continual bits on LED interface.

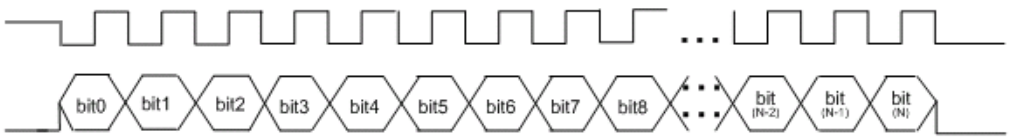

Figure 6-1 : LED Interface Timing and Encoding Explanation

6.8.1 LED Interface Signals

9064 provides 2 sets of LED interfaces according to SmartPort™ Group. The LED interface signals are given as bellow:

Table 6-8 : LED Interface Signals

Name	IO	Description
LED_CLK	O, CMOS	LED Clock
LED_DATA	O, CMOS	Encoded bit stream to drive LED

6.8.2 LED Bit Stream Encode Modes

In order to maximize the facility of driving LED under different application scenario, total ten LED bit stream encode modes are supported in 9064 this could save the external glue logic and only the shift logic is needed.

Table 6-9 : LED Bit Stream Encode Modes

Mode #	Mode Description	On/Off	Blink
0	RX Link	RX Link = 1/0	0
1	TX Link (10GE only)	TX Link = 1/0	0
2	RX Link and activity	RX Link = 1/0	RX activity
3	TX Link and Activity (10GE only)	TX Link = 1/0	TX activity
4	RX Link and RX/TX activity	RX Link = 1/0	RX or TX activity
5	TX activity	0	TX activity
6	RX activity	0	RX activity
7	RX/TX activity	0	RX or TX activity
8	LED Force On	1	0
9	LED Force Off	0	0

So, there are one pair of 2bits (total 4 bits) stand for the LED mode. For example, if user wants LED to be configured to work at mode #2 (Rx Link and activity), LED On/Off mode encode should be 2'b01, LED blink mode encode should be 2'b01.

The LED control are 2 bits, which are deduced from the LED On/Off mode and LED blink mode encoding, LED_PortStatus[1:0] MSB bit is blink bit, 1'b1 is blinking, 1'b0

is Non-blinking; on the other hand, LED_PortStatus[1:0] LSB bit is On/Off bit, 1'b1 is On, 1'b0 is Off. Besides, the MSB bit (i.e. the LED blinking bit) has the higher priority than LSB bit.

Take LED mode #2 as an example:

1. Cfg LED On/Off mode encode = 2'b01, LED blink mode encode= 2'b01;
2. If sample the Rx Link status = 1, then set LED_PortStatus[0]= 1'b1; If sample the Rx activity status = 1, then set LED_PortStatus[1]= 1'b1.
3. Since LED_PortStatus[1:0]= 2'b11, and blink status has the higher priority, the LED refresh bit stream will be 0 => 1 => 0 => 1 toggling according to the interval of LED refresh.

The LED blink behavior is implemented through the "and" operation of BLINK square-wave and the BLINK bit of LED_PortStatus.

If need secondary LED for one port, such as 10GE port, the primary LED displays "Rx Link and activity" (LED mode #2), and the secondary LED displays "TX Link and activity" (LED mode #3), then an extra LED port status bits are required.

Note that if the customer needs all of the MACs' raw link and activity status to be output for further processing (LedRawStatusCfg.rawStatusEn), all of the MACs' mode configuration are not effective.

7 Pin Information

Note[1]: PU/PD is internal Pull Up or Pull Down of LVCMOS IO, the internal pull-up resistor ranges from 35 KΩ to 65KΩ (typical value is 50K kΩ) while the internal pull-down resistor ranges from35KΩ to 65 KΩ (typical value is 50K kΩ)

Note[2]: If not indicate specifically, LVCMOS is 1.8V (typ) IO

Note[3]: “I”/”O”/”B” in Type column represent “Input”/”Output”/”Bi-Direction” respectively.

Note[4]: “OD” is open-drain IO, external pull-up resistor should be used, “PP” is Push-Pull IO

Note[5]: Support 1.8/1.5/1.2V I/O, the recommended frequency is 0~200MHz.

Table 7-1 : Pin information –Function Signals

Pin Name	Type	Rate	Pin #	PU/ PD	Description
SerDes Interface					
HSS_REFCLK_P HSS_REFCLK _N	I LVDS	156.25MHz	2	-	SerDes reference clock.

Pin Name	Type	Rate	Pin #	PU/ PD	Description
CS[00:07]_RXP[7:0] CS[00:07]_RXN[7:0]	I CML	10.3125Gbps ~ 112.5Gbps	128		10.3125G~112.5Gbps SerDes links input Typical configurations are: • XFI/SFI/10GBASE-KR/10.3125Gbps • XLAUI/40GBASE-KR4/CR4 • 25GAUI/25GBASE-KR/CR,25.78125Gbps • 50GAUI-2/50GBASE-CR2/KR2, 25.78125Gbps/26.5625 (NRZ) • 100GBASE-CR4/KR4/CAUI-4, 25.78125Gbps/26.5625 (NRZ) • 50GAUI-1/50GBASE-CR/KR,53.125 (PAM4) • 100GAUI-2/100GBASE-CR2/KR2, 53.125Gbps (PAM4) • 100GAUI-1/100GBASE-CR/KR, 106.25Gbps (PAM4) • 200GAUI-4/200GBASE-CR4/KR4, 53.125Gbps (PAM4) • 200GAUI-2/200GBASE-CR2/KR2, 106.25Gbps (PAM4) • 400GAUI-8/400GBASE-CR8/KR8, 53.125Gbps (PAM4) • 400GAUI-4/400GBASE-CR4/KR4, 106.25Gbps (PAM4) • 800GAUI/800GBASE-KR8/CR8
CS[00:07]_TXP[7:0] CS[00:07]_TXN[7:0]	O CML	10.3125Gbps ~ 112.5Gbps	128		10.3125G~112.5Gbps SerDes links output
PCIe SerDes Interface					
PCIE_REFCLK_P PCIE_REFCLK_N	HCSL	100MHz	2	-	PCIe input deferential reference clock 100M.
PCIE_RXP[3:0] PCIE_RXN[3:0]	I CML	2.5G/ 5G/ 8G	8	-	PCIe input data.

Pin Name	Type	Rate	Pin #	PU/ PD	Description
PCIE_TXP[3:0] PCIE_TXN[3:0]	O CML	2.5G/ 5G/ 8G	8	-	PCIe output data.
PCIE_FORCE_RATE[1:0]	I LVCMOS	Static	2	PD	PCIe force mode: 2'b00: No Force mode; 2'b01: Force to Gen1; 2'b10: Force to Gen2; 2'b11: Force to Gen3;
PCIE_FORCE_WIDTH[1:0]	I LVCMOS	Static	2	PD	PCIe Force Width 2'b00:x4(default); 2'b01: x1; 2'b10:x2; 2'b11: the same as 2'b00
Boot Configuration					
RST_CORE_B	I LVCMOS	Static	1	PD	Chip global reset, active low
FUSE_GO	I LVCMOS	Static	1	PD	Start fuse, active high
FUSE_OK	O LVCMOS	-	1	PD	If assert, indicate the fuse download procedure is finished and procedure is passed.
FUSE_DONE	O LVCMOS	-	1	PD	If assert, indicate the fuse download procedure is finished.
BOOT_GO	I LVCMOS	Static	1	PD	Boot start, load part number
BOOT_DONE	O LVCMOS	-	1	PD	If assert, indicate the boot download procedure is finished.
CFG_PLL_SUP_BYP	I LVCMOS	DC	1	PD	If set, the internal PLL SUP will be bypassed, should tie to GND while bring up
CFG_PLL_CORE_DP_BYP	I LVCMOS	DC	1	PD	If set, the internal CORE DP PLL will be bypassed, should tie to GND while bring up
CFG_PLL_CORE_PP_BYP	I LVCMOS	DC	1	PD	If set, the internal CORE PP PLL will be bypassed, should tie to GND while bring up
BOOT_TEST_MODE	I LVCMOS	DC	1	PD	0: Function Mode 1: Internal DFT Test Mode

Pin Name	Type	Rate	Pin #	PU/ PD	Description
BOOT_ATE_TEST_EN	I LVCMOS	DC	1	PD	0: Function mode 1: ATE Test mode
QSPI_MODE_SEL	I LVCMOS	DC	1	PD	Select QSPI_DATA's valid bits' width. 0: 1 bit is valid 1: 4 bits are valid
QSPI_CLK_DIV_SEL	I LVCMOS	DC	1	-	If QSPI_CLK_DIV_SEL = 0, the Clock Frequency of QSPI is 5.9375MHz. Else, the Clock Frequency is 23.75MHz.
BOOT_I2C_SA[1:0]	I LVCMOS	DC	2	PD	I^2C slave address.
SVB[3:0]	O LVCMOS	DC	4	-	Chip Speed Notification pin
BOOT_PCIE_AUTO_MODE	I LVCMOS	Static	1	PD	Reserve
GPIO Interface					
GPIO[7:0]	B LVCMOS 1.8V	0-200MHz	8	PD	General purpose IO. Could be configured by internal ECPU.
QSPI					
QSPI_CLK	O LVCMOS	25MHz	1	-	QSPI output clock
QSPI_CSB[1:0]	O LVCMOS	Static	2	-	Chip Selection signal of QSPI interface
QSPI_DATA[3:0]	B LVCMOS	25MHz	4	-	QSPI bidirectional data
UART Interface					
UART_TXD[1:0]	O LVCMOS	5MHz	2	-	Tx Data of UART interface UART0 is for MCU, UART1 is for ECPU, also used as TOD_CODE in TsEngine, while UART_TXD1 is used as the output of TOD_CODE.
UART_RXD[1:0]	I LVCMOS	5MHz	2	PU	Rx Data of UART interface UART0 is for MCU, UART1 is for ECPU, also used as TOD_CODE in TsEngine, while UART_RXD1 is used as the input of TOD_CODE.
CORE reference clock					

Pin Name	Type	Rate	Pin #	PU/ PD	Description
CORE_REFCLK_P CORE_REFCLK_N	I LVDS	100MHz	2	-	Differential input reference clock for Core PLL, typical 100MHz
I²C Slave Interface					
SCL	I OD	0-400KHz	1		I²C slave SCL input ,which is used for switch core clcok by I²C interface.
SDA	B OD	0-400KHz	1		I²C slave SDA ,which is used for switch core for data transfer by I²C interface.
SCL_RSV[1:0]	I PP	0-3.4MHz	2		For debug use only
SDA_RSV[1:0]	B PP	0-3.4MHz	2		For debug use only
I²C Master Interface					
MSCL[1:0]	O OD	0-400KHz	2		I²C Master SCL out, up to 400KHz, default is 100KHz
MSDA[1:0]	B OD	0-400KHz	2		I²C Master SDA, related with MSCL0~1.
SMI Interface					
MDC_A[3:0]	O LVCMOS 1.2V/1.8V	0-25MHz	4	-	External PHY MDIO clock, compatible with 1G/10G PHY
MDIO_A[3:0]	BLVCMOS 1.2V/1.8V	0-25MHz	4	-	External PHY MDIO data, compatible with 1G/10G PHY
MDC_B[3:0]	O LVCMOS 1.2V/1.8V	0-25MHz	4	-	External PHY MDIO clock, compatible with 1G/10G PHY
MDIO_B[3:0]	BLVCMOS 1.2V/1.8V	0-25MHz	4	-	External PHY MDIO data, compatible with 1G/10G PHY
LED Interface					
LED_CLK	O LVCMOS	1-100MHz	1	PD	Led clock out.
LED_DATA	O LVCMOS	25MHz	1	PU	Led data out.
Debug Interface					
DEBUG[7:0]	O LVCMOS 1.8V	0-50MHz	8		Used for chip function debugging; Connect to debug tap on board. debug clock should be divided under 50Mhz

Pin Name	Type	Rate	Pin #	PU/ PD	Description
DEBUG_MODE[3:0]	I LVCMOS 1.8V	-	4	PD	Debug mode selection; Connect to debug tap on board;
IEEE1588 Time Stamp Interface					
PTP_REFCLK_P PTP_REFCLK_N	I LVDS	100MHz	2	-	IEEE1588 Time stamp Engine Differential clock input, the only supported frequencies is 100MHz.
TOD_PULSE	BLVCMOS	0-25MHz	1	PD	Typical 1pps assertion.
SYNC_CLK[1:0]	BLVCMOS	0-25MHz	2	PD	TsEngine sync clock, up to 25MHz.
SYNC_PULSE[1:0]	BLVCMOS	0-25MHz	2	PD	TsEngine sync pulse.
SYNC_CODE[1:0]	BLVCMOS	0-25MHz	2	PD	TsEngine sync code.
Interrupt Interface					
INTR_B[3:0]	O LVCMOS	-	4	PU	Interrupt output signals. Active low.
JTAG Interface					
TCK	I LVCMOS	25MHz	1	PU	JTAG Clock input.
TRST_B	I LVCMOS	25MHz	1	PD	JTAG Test Reset. This signal is active low.
TMS	I LVCMOS	25MHz	1	PU	JTAG Test Mode Select input.
TDI	I LVCMOS	25MHz	1	PU	JTAG Data input.
TDO	O LVCMOS	25MHz	1	-	JTAG Data output.
Test Signals(Reserved Signals)					
DFT_CLK_P	I LVCMOS 1.8v		1	PD	DFT Test
DFT_CLK_N	I LVCMOS 1.8v		1	PD	DFT Test
RESERVE[3:0]	B LVCMOS 1.8v		4	-	Reserved pins

Table 7-2 : Pin information –Power and Ground

Pin Name	Type	Rate	Pin #	Description
Power				
VDD	I 0.75	Core Power	84	VDD core power supply (0.8V-0.85V typ)
VDDO	I 1.8V	IO power supply	14	Supply for 1.8V output buffers

Pin Name	Type	Rate	Pin #	Description
VDD18_LVDS	I 1.8V	LVDS power supply	1	Supply for LVDS 1.8V output buffers
VDD18_EFUSE_0	I 1.8V	EFULSE power supply	1	Supply for EFUSE 1.8V output buffers
VDDO1812	I 1.8V or 1.2V	MDIO_A IO Power	2	MDIO_A IO power supply (1.8V or 1.2V typ)
AVDDL_112G	I (0.75V typ)	112G Serdes Anolog power supply	30	Analog power supply
AVDDH_112G	I (1.2V typ)	112G Serdes Anolog power supply	30	Analog power supply
AVDD12A_TS	I (1.2V typ)	PVT power	1	Analog power supply
PLL_VDDHV	I (1.2V typ)	PLL power	1	PLL power supply
GROUND				
VSS	I	GND	1647	Digital Ground
AVSS0A_TS	I	Analog GND	1	Analog GND for PVT

8 Pin-Map and Pin-Out Table

Refer to the spread sheet in excel format. The related document is 9064_Pinlist.

9 Electrical Specification

9.1 Absolute Maximum Rating

CAUTION

Stress above the specification listed in Table 9-1 may cause permanent damage to the device. Function operation is not guaranteed under or above these conditions. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 9-1 : Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD	Digital Logic Voltage	-0.16	0.825	V
AVDDL_112G	112G Analog Power Supply Pins (AVDD*)	-0.16	0.825	V
AVDDH_112G	112G Analog Power Supply Pins (AVDD*)	-0.3	1.236	V
PLL_VDDHV	PLL AVDD	-0.3	1.26	V
VDDO	Digital IO supply	-0.3	1.98	V
VDDO1812[1]	Supply for 1.2V output buffers (1.8V/1.2V selectable)	-0.3	1.32	V
		-0.3	1.98	V
VDD18_LVDS	1.8V LVDS IO AVDD supply	-0.3	1.949	V
VDD18_EFUSE_0	FUSE programming supply	-0.3	1.89	V
$V_{DV/DT}$	Supply Voltage Slew Rate	-	90	V/ms
T_{ST}	Storage Temperature	-40	125	˚C
HBM	JS-001-2017	-1000	1000	V
CDM	JS-002-2018	-250	250	V

NOTE

Note[2]: Supply for 1.8V/1.2V is selected by MDIO_A_VDDIO_SEL and MDIO_B_VDDIO_SEL pin.

9.2 Recommended Operating Conditions

Recommended operating conditions are values that guarantee correct device operation. If the device is used within the ranges, electrical characteristics (DC and AC characteristics) are guaranteed.

Table 9-2 : Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Tolerance (AC+DC)	Unit
VDD	Digital Logic Voltage (VDD)	0.7275 (0.8-3%)	0.75	0.7725 (0.85+3%)	DC: ±1% AC: ±2%	V
AVDDL_112G [1]	Analog Power Supply Pins (AVDD*)	0.7275 (0.8-3%)	0.75	0.7725 (0.85+3%)		V
AVDDH_112G [2]	Analog Power Supply Pins (AVDD*)		1.2	1.236 (1.2+3%)		V
PLL_VDDHV	Other IP Analog Power Supply (AVDD)	1.164	1.2	1.236	±3%	V
VDDO	Digital IO supply	1.746	1.8	1.854	±3%	V
VDD1812	SMI power supply	1.746/1.164	1.8/1.2	1.854/1.236	±3%	
VDD18_LVDS	1.8V LVDS IO AVDD supply	1.746	1.8	1.854	±3%	V
VDD18_EFUSE_0	FUSE programming supply	1.746	1.8	1.854	±3%	V
Tj	Junction Temperature	0		105		˚C
Ta	Ambient operating temperature range	0		70		˚C

NOTE

Note: All voltages are probed from package BGA BALL and the bandwidth is 20MHz.

Note[1]: AC_LO:Peak to Peak AC Nois <30mV from 1kHZ-5Mhz;AC_HI:Peak to Peak AC Nois <15mV from 5MHZ-5Mhz;

Note[2]: AC_LO:Peak to Peak AC Nois <30mV from 1kHZ-5Mhz;AC_HI:Peak to Peak AC Nois <15mV from 5MHZ-5Mhz;Note[3]: The device allows a junction temperature excursion of up to 115˚C for a maximum period of 15 days per year (<88 hours continuous). The excursion temperature may have an increased effect on EM and the performance may degrade.

9.3 Power-Up and Power-Down Specifications

Table 9-3 Power Up and Power Off Timing Parameters

Symbol	Description	Min	Max	Units
tDELAY1	VDD18/1.8V or AVDD12A_TS/1.2V power up to VDDM/0.75V power up delay	1	-	ms
	VDDM/0.75V power off to VDD18/1.8V or AVDD12A_TS/1.2V power off			
tDELAY2	VDDM/0.75V power up to Other 0.75V or VDDH/1.2V power up delay	1	-	ms
	Other 0.75V or VDDH/1.2V power off to VDDM/0.75V power off			

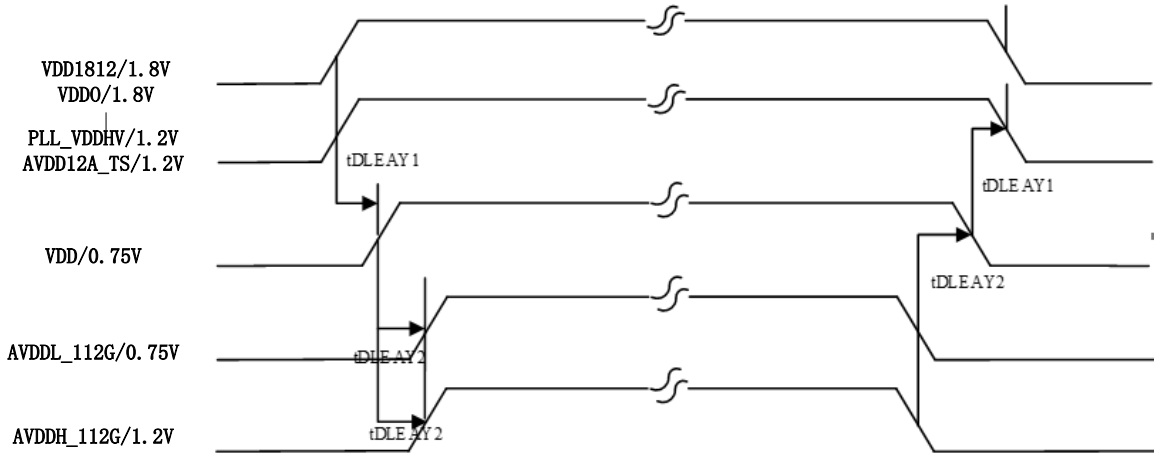

Figure 9-1 Power Up and Power Off Timing

Generally, there is no strict requirement of power off timing. To system design level, users just need to make sure that another round of power-up procedure must be started only after all the power-supply is turn off in the last round.

9.4 Boot Up/Reset Sequence

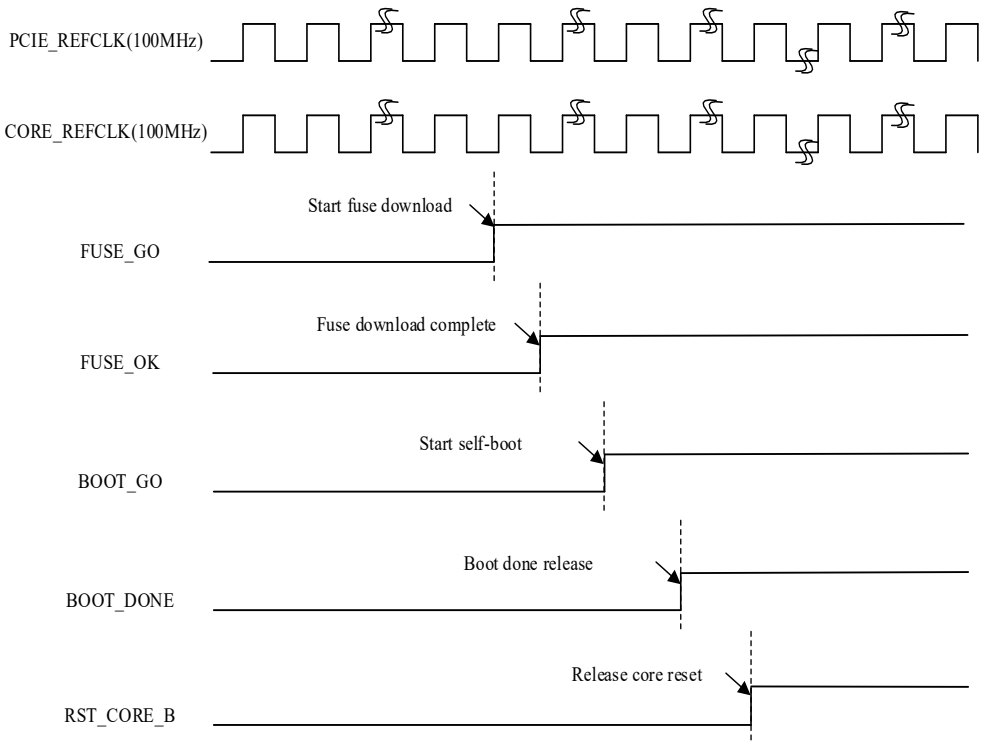

Figure 9-2 : Boot-up sequence

9.5 Power Supply and Power Consumption

Table 9-4 : Maximum Power Consumption (Tj=105℃, TT Corner)

Mode	I/O BW	Freq. (MHz)	Current (A)				VDDIO1V8 (1.8V)	Max (Watts)
			DVDD_Core (0.75V)		AVDDL_112 (1.2V)	AVDDH_112 (1.2V)		
64x100G	6.4T	1.35G/ 1.4G	115		14.5	20	2	125

Table 9-5 : Maximum Power Consumption (Tj=105℃, FF Corner)

Mode	I/O BW	Freq. (MHz)	Current (A)				VDDIO1V8 (1.8V)	Max (Watts)
			DVDD_Core (0.75V)		AVDDL_112 (1.2V)	AVDDH_112 (1.2V)		
64x100G	6.4T	1.35G/ 1.4G	120		23	22	2	135

Table 9-6 : Typical Power Consumption (Tj=75℃, TT Corner))

Mode	I/O BW	Freq. (MHz)	Current (A)				VDDIO1V8 (1.8V)	Typcal (Watts)
			DVDD_Core (0.75V)		AVDDL_112 (1.2V)	AVDDH_112 (1.2V)		
64x100G	6.4T	1.35G / 1.4G	95		14.5	20	2	109

For PSU and thermal designing, the following power requirement for different voltage rails are provided based on 96x100G+64x50G or 128x100G , total 12.8Tbps, other configuration mode could use different number proportionally.

Table 9-7 : Power Requirement for Different Voltage rail

Power	Typical Voltage Unit: V	Current(Max.) Unit: A
VDD	0.75	120
AVDDL_112G [1]	0.75	22
AVDDH_112G [1]	1.2	20
PLL_PLLAVDD12	1.2	0.1
VDDO	1.8	2
VDD1812	1.8	0.1
VDD18_LVDS	1.8	0.1
VDD18_EFUSE_0	1.8	0.1
VDD		

9.6 Interface I/O DC Specifications

9.6.1 QSPI/MDIO/ LED I/O Specifications

Table 9-8 : 1.8V MODE IO driver/receiver dc specification (VDDO = 1.8V)

Symbol	Parameter	Min	Typ.	Max	Units
VDD	IO power supply	1.62	1.80	1.98	V
V_{IL}	DC Input Logic Low	-0.400	-	VDDO*30%	V
V_{IH}	DC Input Logic High	VDDO*70%	-	VDDO+0.4	V
V_{OL}	DC Output Logic Low	-	-	0.4	V
V_{OH}	DC Output Logic High	VDDO-0.4	-	-	V
C_I	Input capacitance			5	pF
I_I	Input Leakage Current VDDO is ON, 0<V(PAD)<VDDO			10	uA

Symbol	Parameter	Min	Typ.	Max	Units
I_{OL}	Low Level Output Current @V_{OL} (0.4V)	3.7	16.5	-	mA
I_{OH}	High Level Output Current @V_{OH} (VDDO-0.4V)	3.7	16.5		mA
Freq.	IO frequency			200	MHz

Table 9-9 : 1.2V MODE LVCMOS IO DC specification (VDDO = 1.2V)

Symbol	Parameter	Min	Typ.	Max	Units
VDDO	IO power supply	1.08	1.20	1.32	V
V_{IL}	DC Input Logic Low	-0.400	-	VDDO*30%	V
V_{IH}	DC Input Logic High	VDDO*70%	-	VDDO+0.4	V
V_{OL}	DC Output Logic Low	-	-	0.2	V
V_{OH}	DC Output Logic High	VDDO-0.2	-	-	V
I_{OL}	Low Level Output Current @V_{OL} (0.2V)	1.4	8.0	-	mA
I_{OH}	High Level Output Current @V_{OH} (VDDO-0.2V)	1.4	8.0		mA
Freq.	IO frequency			300	MHz

9.6.2 I²C Specifications

Table 9-10 : 1.8V MODE LVCMOS I/O receiver dc specification

Symbol	Parameter	Min	Typ.	Max	Units
VDDO	IO power supply	1.62	1.80	1.98	V
V_{IL}	DC Input Logic Low	-0.400	-	VDDO*30%	V
V_{IH}	DC Input Logic High	VDDO*70%	-	1.98	V
V_{OL}	DC Output Logic Low	-	-	0.4	V
V_{OH}	DC Output Logic High	VDDO-0.4	-	-	V
C_I	Input capacitance			5	pF
I_I	Input Leakage Current VDDO is ON, 0<V(PAD)<VDDO			10	uA
I_{OL}	Low Level Output Current @V_{OL} (0.4V)	3.7	16.5	-	mA
I_{OH}	High Level Output Current @V_{OH} (VDDO-0.4V)	3.7	16.5		mA
T_{rise}	100pF<C_{load}<400pF	25		250	ns
T_{fall}	100pF<C_{load}<400pF	25		250	ns
C_b	Capacitive load bus line			400	pF

Symbol	Parameter	Min	Typ.	Max	Units
Clock frequency	IO frequency			400	KHz

9.6.3 HSS112G SerDes Electrical Specifications

Unless special permission, Table 9-11 characteristics should be satisfied while operating within the Normal Range of Operating conditions. These specifications will be applied on 9064 BGA balls.

Table 9-11 : HSS112G SerDes Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ.	Max	Units
Vdiff-out	Output Differential Voltage Range	Programmable	400		1200	mVp-p
VCM_TX	Output Common Mode Voltage		0.4	0.43	0.6	V
VCM_RX	Input Common Mode Voltage			372.5		V
Vdiff-in	Input differential Voltage		0	900	1200	mVp-p
R_RX	RX Input Resistance		72	90	108	Ohm

10 AC Timing

10.1 Clock Source Supply

Table 10-1 : Characteristics of chip interface reference clock

Seq#	Signals	Description	Freq.Typ (MHz)	Requirement
1	CORE_REFCLK_P/N[1]	Core reference clock	100	Freq Accuracy: 50ppm Duty cycle: 45%-55% Differential input swing: 0.4-1.6V
2	HSS_REFCLK_P/N[2]	Ext reference clock for Slice0/1	156.25	Duty cycle: 45%-55% Rise/Fall time(20-80%):0-0.6ns Single-ended amplitude: 0.2-0.8V
3	PCIE_REFCLK_P/N	PCIe reference clock	100	[3]
4	PTP_REFCLK_P/N	PTP reference clock for IEEE1588	100	Freq Accuracy: 50ppm[4] Duty cycle: 45%-55% Differential input swing: 0.4-1.6V

NOTE

Note[1]: CORE and PTP reference clock requirements refer to the Table 10-4.

Note[2]: HSS112G SerDes reference clock requirements refer to the 错误!未找到引用源。.

Note[3]: PCIe 100MHz reference clock requirements refer to the Table 10-3 PCIe SIG spec.

Note[4]: If use SyncE, Frequency tolerance is ±4.6ppm.

Table 10-2 HSS112G SerDes External Reference Clock Requirements

Symbol	Parameter	Conditions	Min	Typ.	Max	Units
CLKPNM	Phase Noise Mask	@10khz, for ref clock frequency at 156.25Mhz	-123			dBc/Hz
		@50khz, for ref clock frequency at 156.25Mhz	-124			dBc/Hz
		@100khz, for ref clock frequency at 156.25Mhz	-127			dBc/Hz

Symbol	Parameter	Conditions	Min	Typ.	Max	Units
		@500khz, for ref clock frequency at 156.25Mhz	-146			dBc/Hz
		@1Mhz, for ref clock frequency at 156.25Mhz	-151			dBc/Hz
		@5Mhz, for ref clock frequency at 156.25Mhz	-152			dBc/Hz
		@10Mhz, for ref clock frequency at 156.25Mhz	-152			dBc/Hz
CLKIDC	Clock Input Duty Cycle		45	-	55	%
CLKIRF	Clock Input Rise/Fall Time(20 to 80%)				1280	ps
CLKOFFSET	Reference Clock Accuracy		-50		50	ppm
	Single-ended amplitude					mv
	Voltage Format	LVDS or LVPECL				

Table 10-3 : PCIe Reference Clock Jitter and Swing Requirement

Application	Reference Clock Jitter and Swing Requirement
PCIe 2.5 Gbps	For requirements, refer to the PCI Express 1.0 Card Electrometrical specification
PCIe 5.0 Gbps	For requirements, refer to the PCI Express 2.0 base specification
PCIe 8.0 Gbps	For requirements, refer to the PCI Express 3.0 base specification

Table 10-4 : CORE Reference Clock Requirements

Symbol	Parameter	Conditions	Min	Units
CLKPNM	Phase Noise Mask	@1khz, for ref clock frequency at 100Mhz	-104	dBc/Hz
		@10khz, for ref clock frequency at 100Mhz	-114	dBc/Hz
		@100khz, for ref clock frequency at 100Mhz	-124	dBc/Hz
		@1Mhz, for ref clock frequency at 100Mhz	-134	dBc/Hz
		@10Mhz, for ref clock frequency at 100Mhz	-144	dBc/Hz

10.2 Recovery Clock Output

Table 10-5 : SerDes Recovery Clock Output Frequency

Serdes Data Rate (Gbps)	Serdes Signaling	Serdes Clock(MHz)	Protocol	SyncE Output (KHz)
106.25	PAM4	830.078125	KR8, CR8, 400GAUI-8	976.5625
53.125	PAM4	830.078125	KR8, CR8, 400GAUI-8	976.5625
51.5625	PAM4	805.6640625	KR2, CR2, 100GAUI-2	976.5625
26.5625	NRZ	830.078125	KR4, CR4, 100GAUI-4	976.5625
25.78125	NRZ	805.6640625	KR4, CR4, CAUI-4	976.5625
10.3125	NRZ	322.265625	KR4, CR4, XLAUI	976.5625

10.3 I²C Interface Timing Parameter

Table 10-6 : Characteristics of the SDA and SCL for S-mode[1],from THE I2C-BUS SPECIFICATION

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		Units
		MIN.	MAX.	MIN.	MAX.	
SCL Clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time(repeated) START condition. After this period, the first clock pulse is generated	$t_{HD,STA}$	4.0	—	0.6	—	μs
LOW period of SCL clock	t_{LOW}	4.7	—	1.3	—	μs
HIGH period of the SCL clock	t_{HIGH}	4.0	—	0.6	—	μs
Set-up time for a repeated START condition	$t_{SU,STA}$	4.7	—	0.6	—	μs
Data hold time: for CBUS compatible masters for I²C-bus devices	$t_{HD,DAT}$	5.0 0[2]	— 3.45[3]	— 0[2]	— 0.9[3]	μs
Data set-up time	$t_{SU,DAT}$	250	—	100[4]	—	ns
Rise time of both SDA and SCL signals	t_r	—	1000	20+0.1C_b[5]	300	ns
Fall time of both SDA and SCL signals	t_f	—	300	20+0.2C_b[5]	300	ns
Set-up time for STOP condition	$t_{SU,STO}$	4.0	—	0.6	—	μs
Bus free time between a	t_{BUF}	4.7	—	1.3	—	μs

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		Units
		MIN.	MAX.	MIN.	MAX.	
STOP and START condition						
Capacitive load for each bus line	C_b	—	400	—	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	0.1VDD	—	0.1VDD	—	V
Noise margin at the High level for each connected device (including hysteresis)	V_{nH}	0.2VDD	—	0.2VDD	—	V

Table 10-7 : Characteristics of the SDAH and SCLH for HS-mode[2], from THE I2C-BUS SPECIFICATION

PARAMETER	SYMBOL	C_b=100pF MAX		C_b=400pF		Units
		MIN.	MAX.	MIN.	MAX.	
SCLH Clock frequency	f_{SCLH}	0	3.4	0	1.7	MHz
Hold time(repeated) START condition. After this period, the first clock pulse is generated	$t_{HD,STA}$	160	—	160	—	ns
LOW period of SCLH clock	t_{LOW}	160	—	320	—	ns
HIGH period of the SCLH clock	t_{HIGH}	60	—	120	—	ns
Set-up time for a repeated START condition	$t_{SU,STA}$	160	—	160	—	ns
Data hold time: for CBUS compatible masters for I^2C-bus devices	$t_{HD,DAT}$	0	70	0	150	ns
Data set-up time	$t_{SU,DAT}$	10	—	10	—	ns
Rise time of SCLH signal	t_{rCL}	10	40	20	80	ns
Rise time of SCLH signal after a repeated START condition and after an acknowledge bit	t_{rCL1}	10	80	20	160	ns
Fall time of SCLH signal	t_{fCL}	10	40	20	80	ns
Rise time of SDAH signal	t_{rDA}	10	80	20	160	ns
Fall time of SDAH signal	t_{fDA}	10	80	20	160	ns
Set-up time for STOP condition	$t_{SU,STO}$	160	—	160	—	ns

PARAMETER	SYMBOL	C_b=100pF MAX		C_b=400pF		Units
		MIN.	MAX.	MIN.	MAX.	
Capacitive load for each bus line	C_b	—	100	—	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	0.1VDD	—	0.1VDD	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	0.2VDD	—	0.2VDD	—	V

NOTE

Note[1]: The specs is referred to “THE I2C-BUS SPECIFICATION”

Note[2]: A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note[3]: The maximum tHD;DAT has only to be met if the device does not stretch the LOW period (tLOW) of the SCL signal.

Note[4]: A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement tSU;DAT ⩾250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + tSU;DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the SCL line is released.

Note[5] Cb = total capacitance of one bus line in pF.

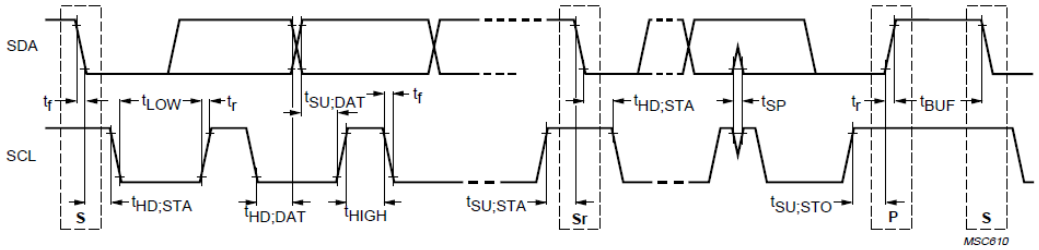

Figure 10-1 : Definition of timing of I^2C

10.4 MDC/MDIO Interface Timing

Table 10-8 : MDC/MDIO Interface Timing Parameters

Symbol	Signals	Description	Min	Max	Units
F_{MDC}	MDC_*	MDC clock frequency	-	25	MHz
DC_{MDC}	MDC_*	MDC clock duty cycle	40	60	%

Symbol	Signals	Description	Min	Max	Units
T_{SU}	MDIO_*	MDIO input Setup time	10	-	nS
T_{HD}	MDIO_*	MDIO input Hold time	0	-	nS
T_{OSU}	MDIO_*	MDIO output Setup time	10	-	nS
T_{OH}	MDIO_*	MDIO output Hold time	10	-	nS

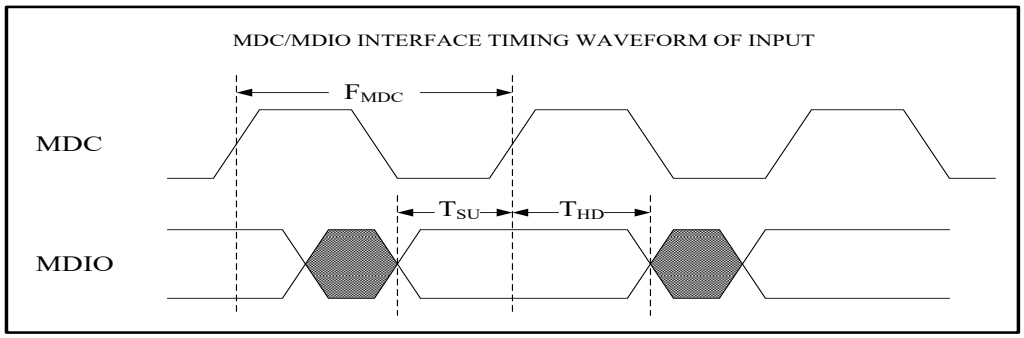

Figure 10-2 : MDC/MDIO Input Timing Diagram

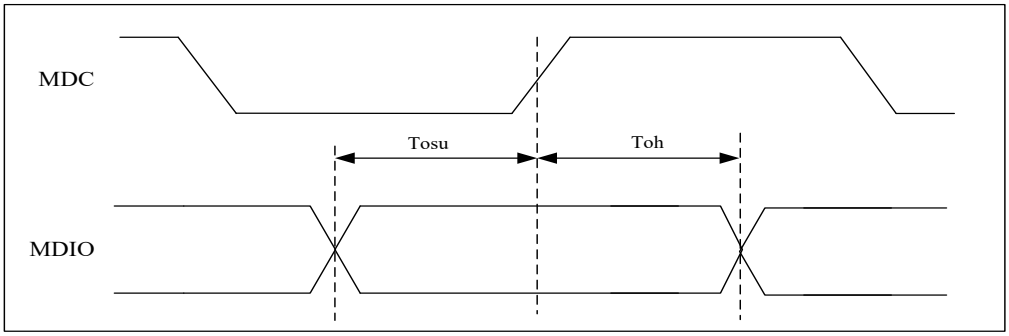

Figure 10-3 : MDC/MDIO Output Timing Diagram

10.5 LED Interface Timing Parameter

Table 10-9 : LED Interface Timing Parameters

Symbol	Signals	Description	Relative to Clock	Min	Max	Units
Freq	LEDCLK	LED clocks	N/A	-	25	MHz
DC	LEDCLK	LED clock duty cycle	N/A	40	60	%
T_{OSU}	MACLED	MACLED output setup time	LEDCLK	10	-	nS
T_{OH}	MACLED	MACLED output hold time	LEDCLK	10	-	nS

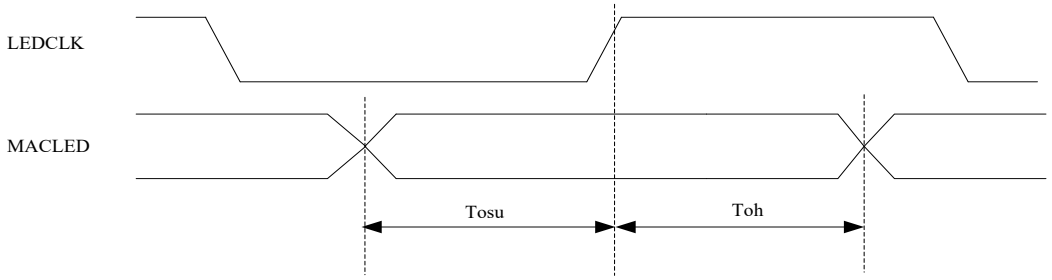

Figure 10-4 : LEDCLK/MACLED Output Timing Diagram

10.6 QSPI Interface Timing Parameter

Table 10-10 : QSPI Interface Timing Parameters

Symbol	Signals	Description	Min	Typ	Max	Units
fCK	QSPI_CLK	QSPI clock frequency	1	-	25	MHz
tCK	QSPI_CLK	QSPI clock period	40	1/tCK	1000	ns
tWH	QSPI_CLK	QSPI clock high time	0.4tCK	-	0.6tCK	nS
tWL	QSPI_CLK	QSPI clock low time	0.4tCK	-	0.6tCK	nS
tDO	QSPI_DATA	QSPI data output valid time	-	-	12	nS
tSU	QSPI_DATA	QSPI data Setup time	5		-	nS
tHD	QSPI_DATA	QSPI data Hold time	5		-	nS
tCSS	QSPI_CS[1:0]	QSPI chip select output lead time	0.5 tCK		-	nS
tCSH	QSPI_CS[1:0]	QSPI chip select output trail time	0.5 tCK		-	nS

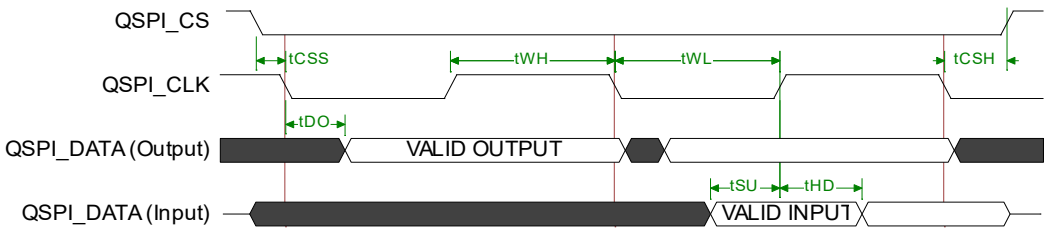

Figure 10-5 : QSPI_* Timing Diagram

11 Thermal Specifications

θja = Junction to Ambient thermal resistance (°C/W)

θjc = Junction to Package Case thermal resistance (°C/W), Case temperature measured at the top center of the outside surface of the component package

θjb = Junction to Board thermal resistance (°C/W). Board temperature measured at the center ball or column location on the outer most ball or column row of the longest side of the package.

The typical θja is 0.5C/W with heat sink and environment as below:

- Heatsink Width in mm ---------->100
- Heatsink Length in mm ---------->200
- Heatsink Height in mm ---------->30
- Air Flow in LFPM ---------->700
- Heat sink Base Thickness in mm ---------->7
- Heat sink Fins Pitch in mm ---------->3.2
- Heat sink Fin Thickness in mm ---------->1.2
- Number of Fins ---------->63
- Thermal Resistance of Heat sink in C/W ---------->0.21 @ 700 LFPM air flow
- Estimated Mass(weight) of Heat sink in grams -------->1680g
- Heat sink Material ---------->Extrusion Grade Aluminum with copper inlay

Air Flow in FPM	200	300	400	600	700	900	1100
θja (C/W)	0.64	0.47	0.39	0.34	0.32	0.29	0.24
θsa (C/W)	0.55	0.367	0.28	0.23	0.21	0.18	0.13

θsa is the thermal resistance of proposed heat sink.

For this package/Die combination:

- θjc = 0.096 Degree C/Watt
- θjb = 0.122 Degree C/Watt

NOTE

- 1. This proposed heat sink solution is a traditional extruded heat sink solution, which meets thermal requirement for a listed application and environment conditions.
- 2. Note that many more other thermal solutions can be possible for this package and application environments.
- 3. The heat sink attaches process uses phase change material with 3.8 W/m-K thermal conductivity, 5mil thickness and at least 80% coverage.
- 4. If any of these application conditions or thermal parameters changes, the thermal solution may not work.

12 Package Mechanical Dimensions

Table 12-1 is the package size description of 9064.

Table 12-1 : Package size

Package Type	Package	Package Dimension	Lead frame	Package thickness (mm) Include BALL	Pin pitch (mm)
FC-PBGA	2197, FC-PBGA	47.5mm*47.5mm	OPL Forced Lead Free	Nom=3.66 Max=3.88	1.0

Figure 12-1 is the 9064 package mechanical diagram.

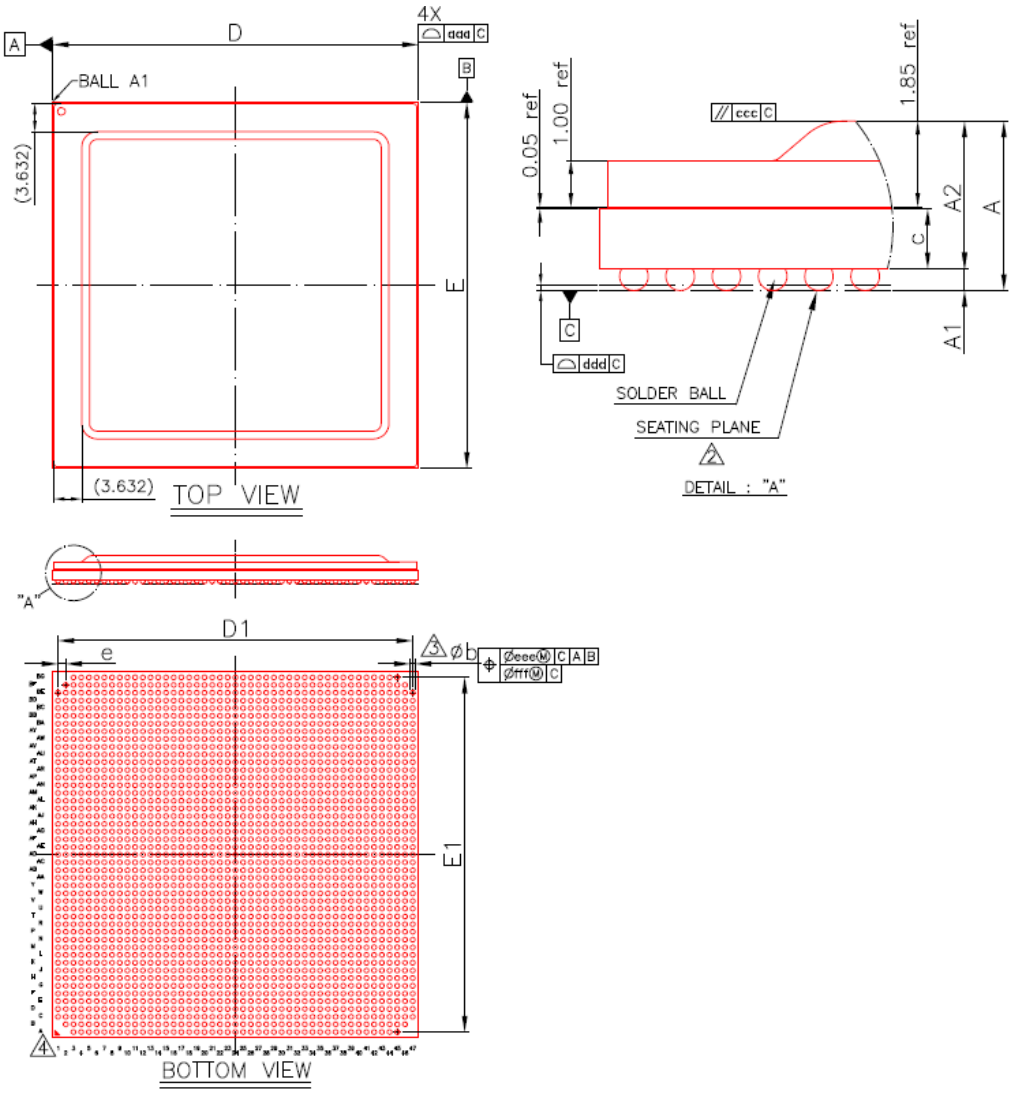

Figure 12-1 : Package Size Parameters

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	3.44	3.66	3.88	0.135	0.144	0.153
A1	0.37	0.47	0.57	0.015	0.019	0.022
A2	2.99	3.19	3.39	0.118	0.126	0.133
C	1.14	1.29	1.44	0.045	0.051	0.057
D	47.30	47.50	47.70	1.862	1.870	1.878
E	47.30	47.50	47.70	1.862	1.870	1.878
D1	---	46.00	---	---	1.811	---

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
E1	---	46.00	---	---	1.811	---
E	---	1.00	---	---	0.039	---
b	0.52	0.62	0.72	0.020	0.024	0.028
aaa	0.20			0.008		
ccc	0.35			0.014		
ddd	0.20			0.008		
eee	0.25			0.010		
fff	0.10			0.004		
MD/ME	47/47					

NOTE

1. CONTROLLING DIMENSION: MILLMETER
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFIEND BY THE SPHERICAL CROWNS OF THE SOLDER BALLS
3. DIMENSION b IS MESURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
5. BALL PLACEMENT USE 0.60 mm SOLDER BALL BGA PAD SOLDER PAD SOLDER MASK OPENING=0.50mm

