9064 Ethernet Switch Silicon Product Brief

- Highly integrated scalable switching for chasis Fabric Lane Card, Large Scale Enterprise and Campus Aggregation/Core chassis solution
- 10GE, 25GE, 40GE, 50GE, 100GE, 200GE, 400G, and 800G interfaces
- Enhanced on-chip Flow Tracing Engine for up to 128K flow table of NetFlow per packet-process engine and MMU engine
- Embedded Traffic manager providing 12 queue per port
- In-band Network Telemetry (INT) and In-band Flow Analyze (IFA) integration for Network Telemetry application
- Support Jumbo Frame up to 9600Bytes
- Improved PFC/WRED and headroom mechanism for lossless Ethernet
- Flexible forwarding database and policy-based table which can be configured to be different memory profile for different application

Application

9064	
√	ToR
	Enterprise Core Switch

Physical facts

9064	64x112G Serdes

OVERVIEW

9064 is a leading purpose-built switch silicon that can be used to build high scalable, feature-rich versatile solution for ToR, Chassis Fabric Lane Card, Large Scale Enterprise and Campus Aggregation/Core chassis. 9064 supports up to 6.4Tbps I/O bandwidth and 2.7 BPPS core bandwidth. 9064 equips with 64 of SerDes Lanes. The device supports 10GE, 25GE, 40GE, 50GE, 100GE, 200GE, 400G, and 800G ports. There are two configuration modes of these 64 serdes lanes, the one is Mode A: 64x112G. The typical form factor of Mode A is 48x100G(R1) + 4x400G(R4) and the typical form factor for Mode B is 16x400G(R4).

FEATURES

- Full set of Layer 2 and Layer 3 protocol
  - VLAN, MAC, LAG, ECMP, Storm Control, VRF, VXLAN, 802.1BR， etc.
  - Per L3 interface L3 protocol packet processing
  - Per VLAN DHCP/ARP handling
  - IPv4 and IPv6 host route
  - Algorithm based IPv4 and IPv6 LPM (TCAM-based lookup is also supported)
  - Loose and strict RPF check
  - IPv6 Based Segment Routing
- IP Overlay
  - VXLAN / NVGRE / VXLAN-GPE / GENEVE Support
- OAM/APS
  - 802.1ag/ Y.1731Ethernet OAM
  - G.8113.1/ G.8113.2 MPLS-TP OAM
  - TWAMP
  - Ethernet/MPLS-TP APS and BFD/ OAM APS
  - monitoring
- Telemetry Feature Set
  - Integrated Counter Sensor, path Sensor and hardware based IPFIX
  - MAC / Enq/Deq / ACL based Stats
  - Buffer Depth Counter and Event Log
  - INT: Standard INT, INT over UDP/TCP
  - INT enabling mechanism: flow based
  - Multi-hop INT insertion capability
  - IFA: support Live Traffic Mode and Clone Mode
  - Hardware Overlay Tunnel Learning
  - Hardware based aging
  - New Flow Export
- Network Time Synchronization
  - IEEE 1588-2008 with up to 4 management domains
  - PTP over Ethernet/IPv4/IPv6

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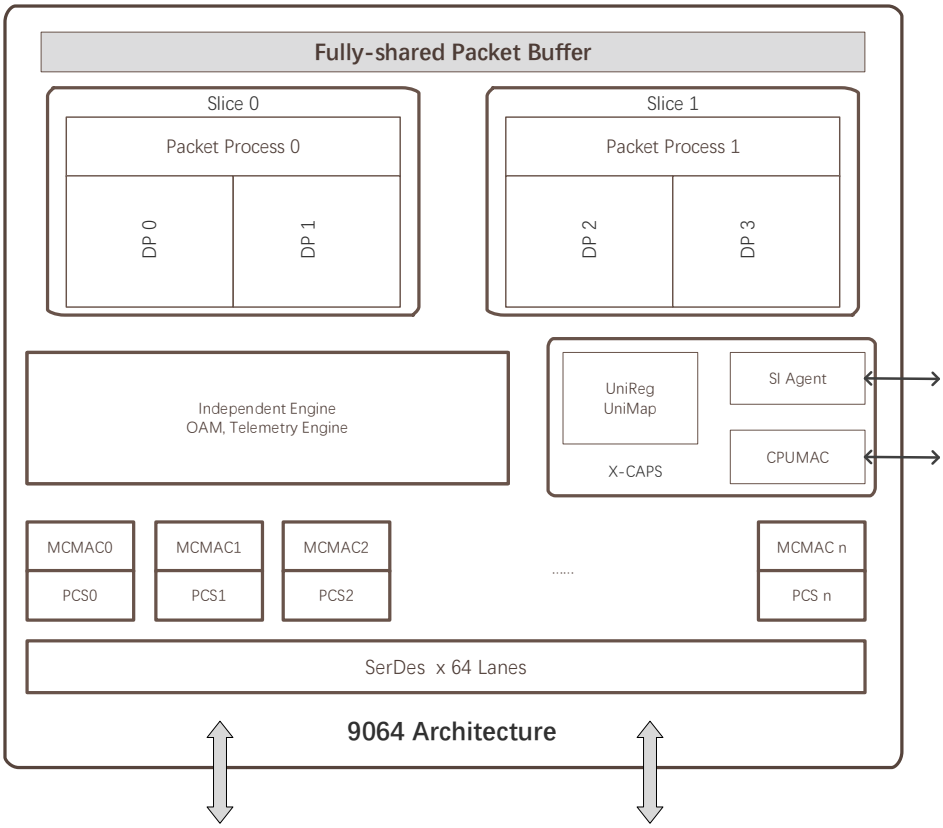
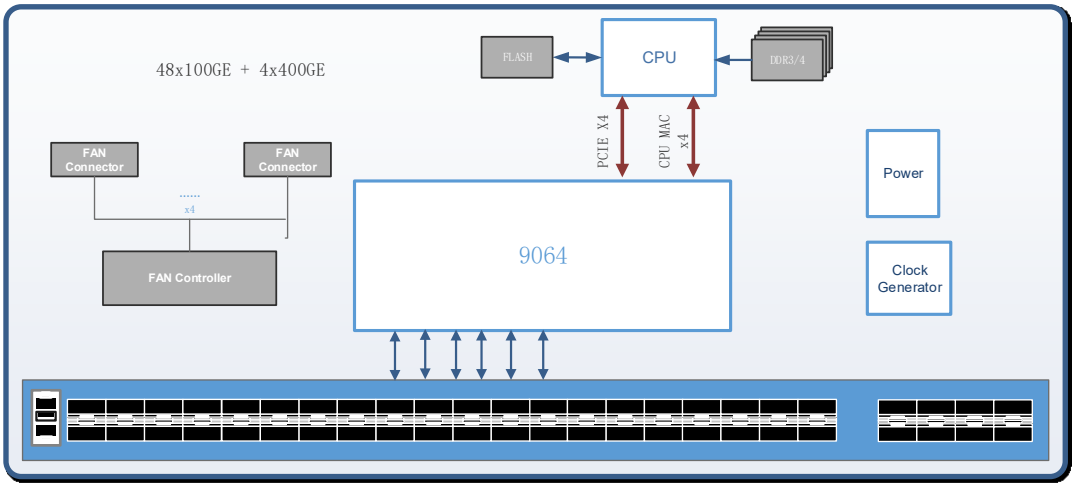
9064 Architecture Diagram



ToR Switch Application



Typical Scenario	Form Factor
ToR Switch	48x100G-R1 + 4x400G-R4